

DJ2 Montevina UMA Schematics Document

uFCPGA Mobile Penryn

Intel GM45+ICH9M

2010-06-02

REV : X00

DY : Nopop Component
HDMI : Pop for HDMI
GIGA : Pop for GIGA LAN
10/100 : Pop for 10/100 LAN

<Core Design>



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Title

Cover Page

Size
A3

Document Number

DJ2 Montevina UMA

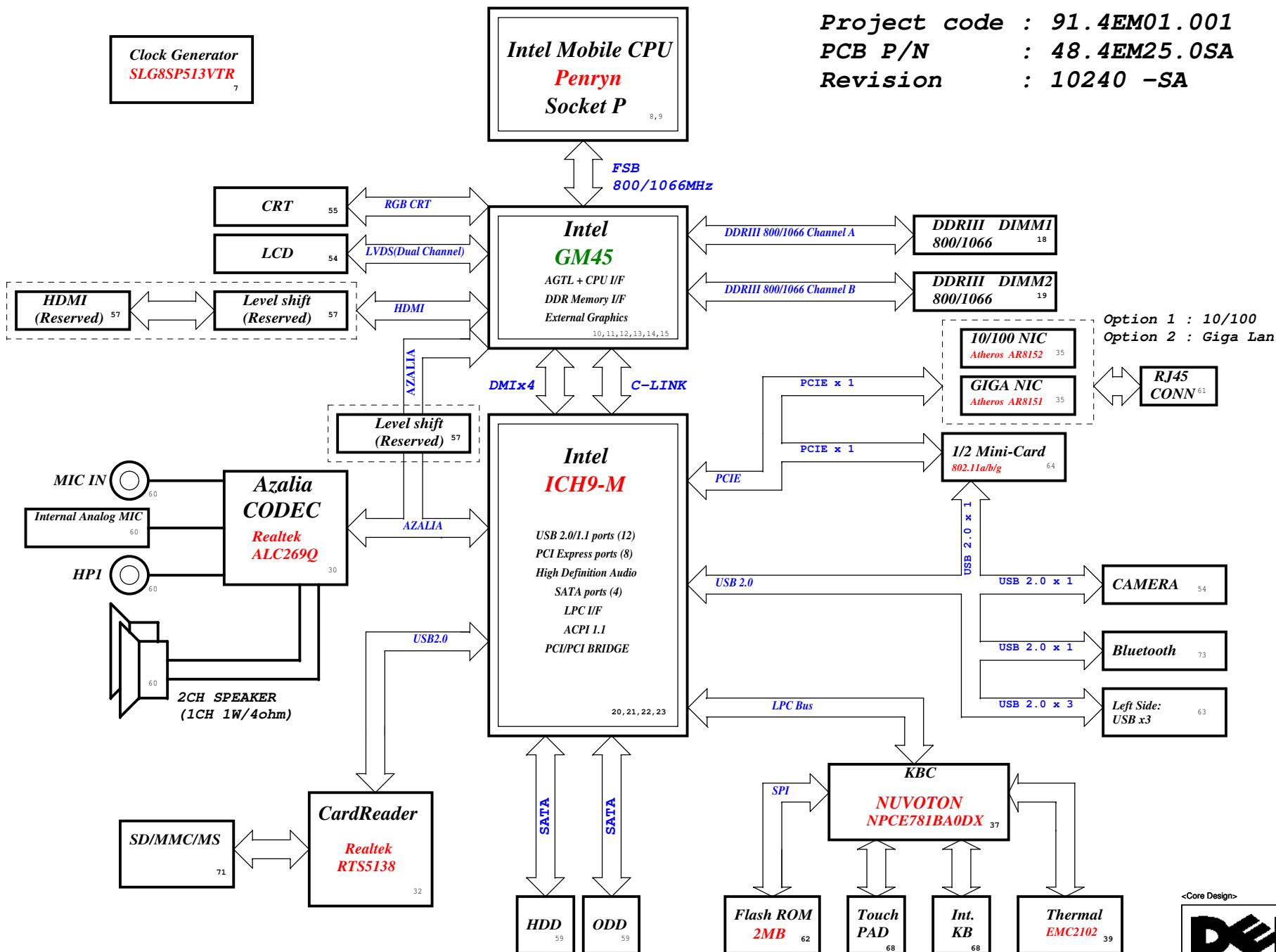
Rev

X00

Date: Wednesday, June 02, 2010

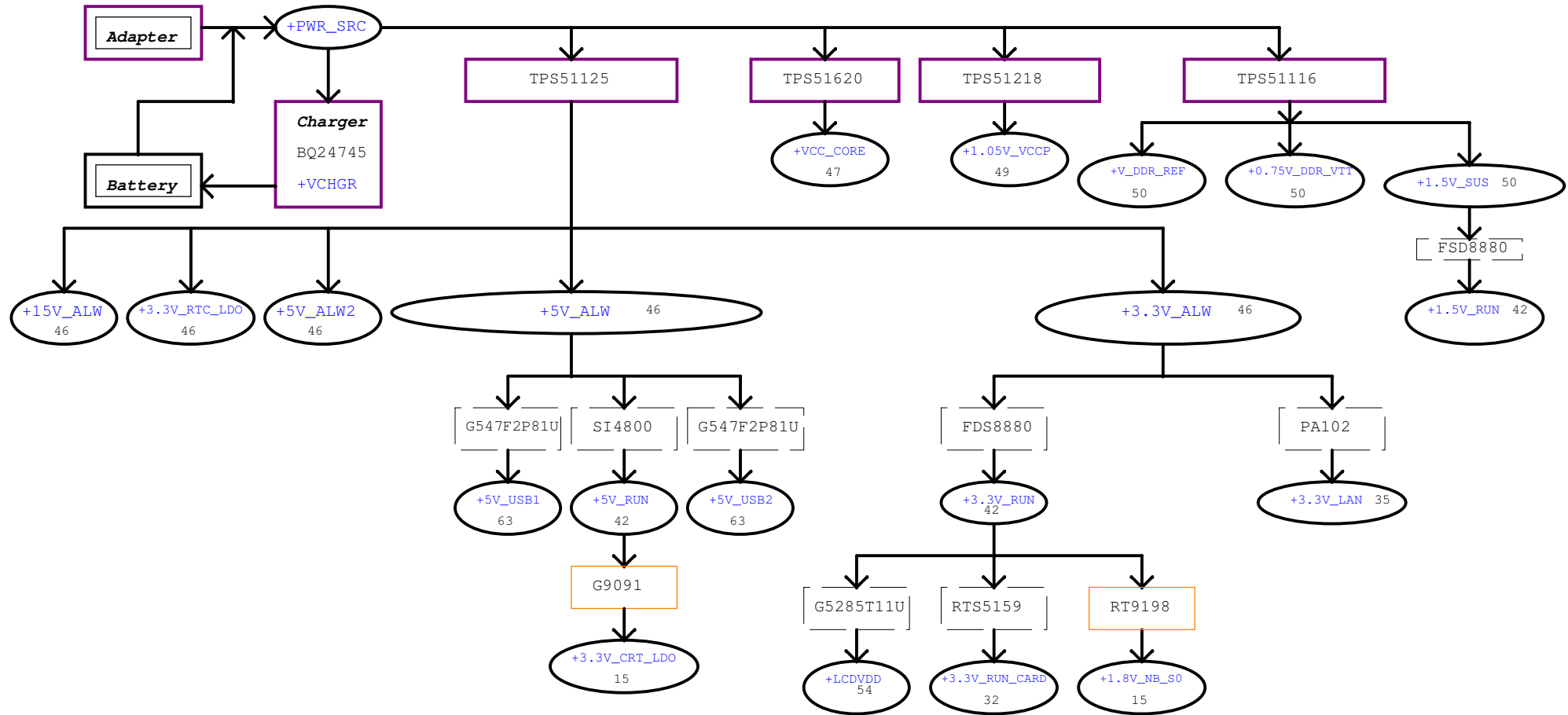
Sheet 1 of 88

Project code : 91.4EM01.001
PCB P/N : 48.4EM25.0SA
Revision : 10240 -SA



CPU DC/DC TPS51620		47
INPUTS	OUTPUTS	
+PWR_SRC	+VCC_CORE	
SYSTEM DC/DC TPS51218		
INPUTS	OUTPUTS	
+PWR_SRC	+1.05V_VCCP	
SYSTEM DC/DC TPS51125		
INPUTS	OUTPUTS	
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW	
SYSTEM DC/DC TPS51116		
INPUTS	OUTPUTS	
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF	
MAXIM CHARGER BQ24745		
INPUTS	OUTPUTS	
+DC_IN +PBATT	+PWR_SRC	
SYSTEM DC/DC Switches		
INPUTS	OUTPUTS	
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN	
PCB LAYER		
L1: Top		
L2: GND		
L3: Signal		
L4: Signal		
L5: VCC		
L6: Bottom		

DJ1 Montevina UMA Power Block Diagram



Power Shape



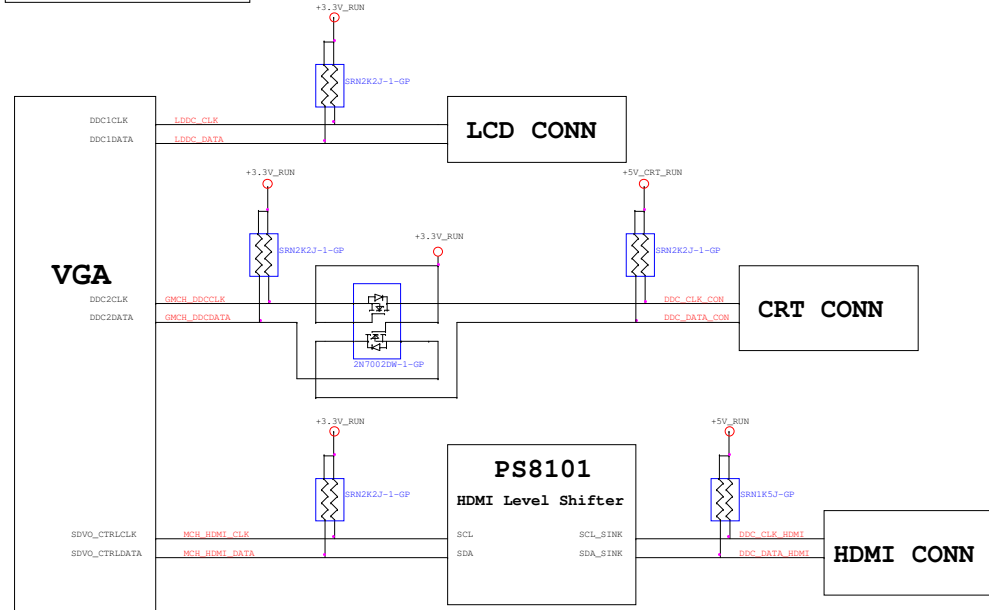
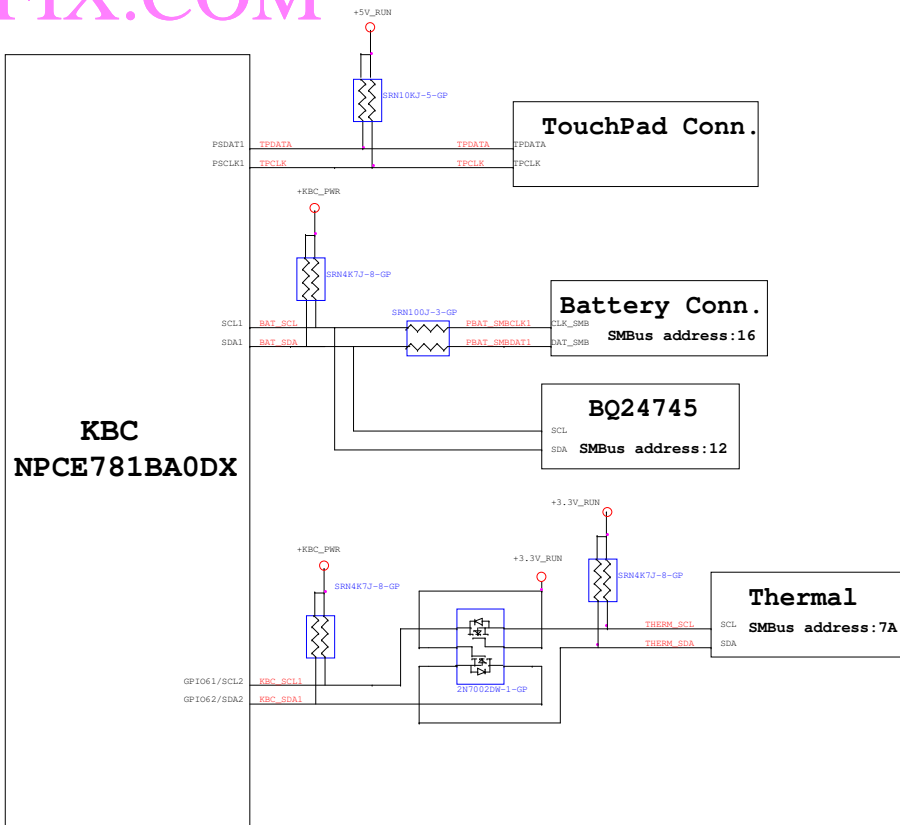
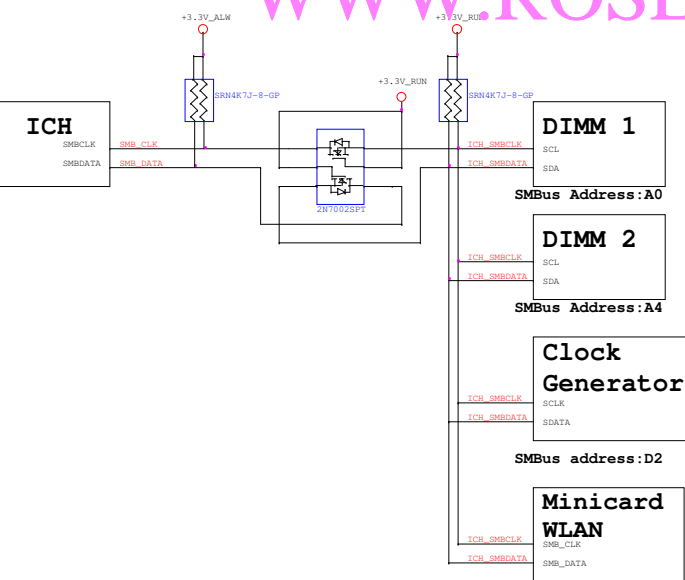
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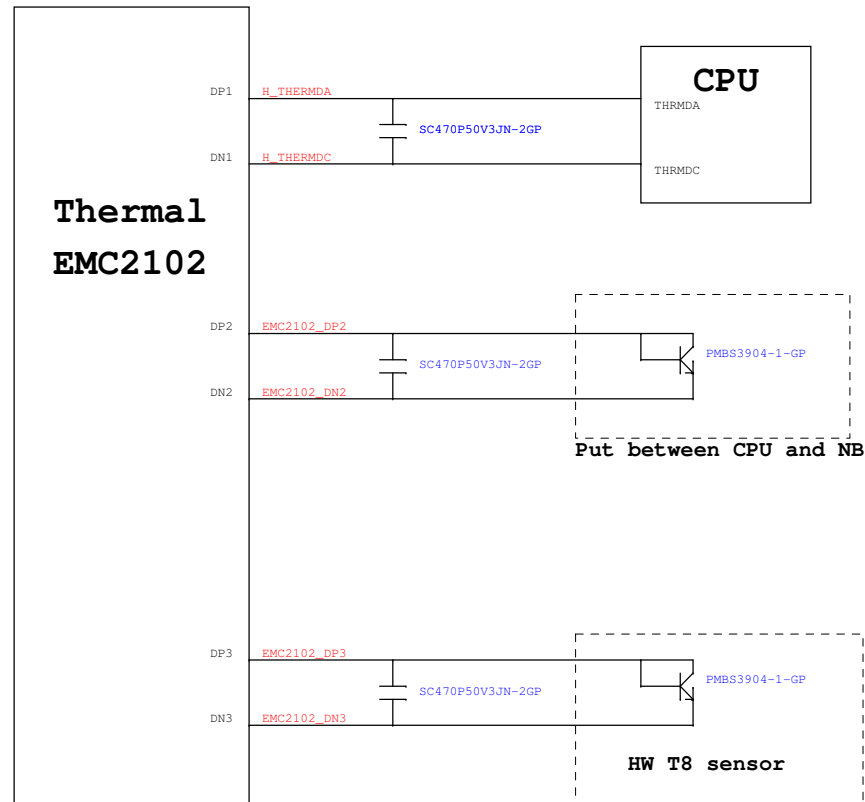
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A3	DJ2 Montevina UMA	Friday, May 28, 2010	X00
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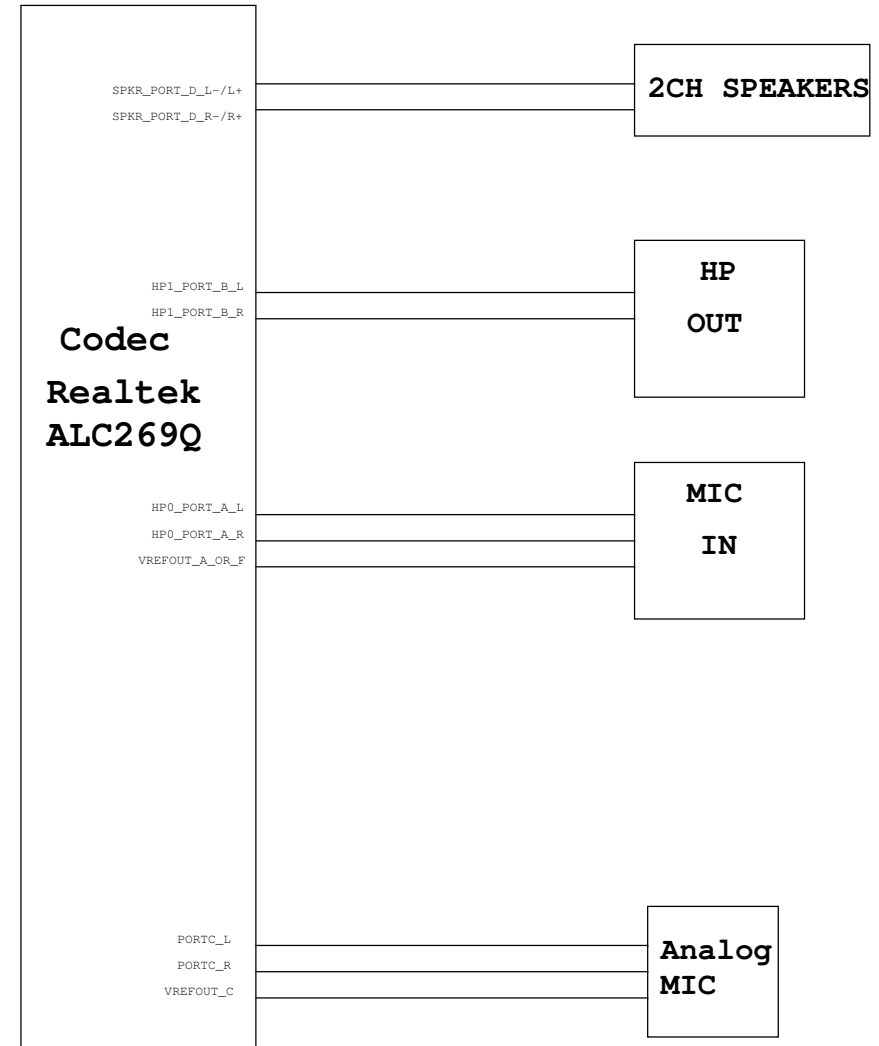
ICH SMBus Block Diagram KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



<Core Design>

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.2.3

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.2.3

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 355648 Rev.2.3

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance / PCI Express* Port Config 1 bit 1 (Port 1-4), Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers: Offset 224h). This signal has a weak internal pull-down.
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4), Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers: Offset 224h).
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6), Rising Edge of PWROK	This signal has a weak internal pull-up. Sets bit 2 of RPC.PC2 (Chipset Config Registers: Offset 0224h) when sampled low.
GPIO20	Reserved, Rising Edge of PWROK	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high
GNT1# / GPIO51	ESI Strap (Server Only), Rising Edge of PWROK.	Tying this strap low configures DMI for ESIncompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3# / GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: this indicates that the system is strapped to the "top-block swap" mode (IntelR ICH9 inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers: Offset 3414h: bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#	Boot BIOS Destination Selection 1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. <div> <div>Bit11 (GNT0#)</div> <div>Bit 10 (SPI_CS1#)</div> <div>Boot BIOS Destination</div> <div> <div>0</div> <div>1</div> <div>1</div> <div>0</div> </div> <div> <div>SPI</div> <div>PCI</div> <div>LPC</div> <div>Reserved</div> </div> </div>
SPI_CS1# / GPIO58	Boot BIOS Destination Selection 0, Rising Edge of CLPWROK	Controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. <div> <div>Bit11 (GNT0#)</div> <div>Bit 10 (SPI_CS1#)</div> <div>Boot BIOS Destination</div> <div> <div>0</div> <div>1</div> <div>1</div> <div>0</div> </div> <div> <div>SPI</div> <div>PCI</div> <div>LPC</div> <div>Reserved</div> </div> </div>
SATALED#	PCI Express Lane Reversal (Lanes 1-4). Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0: Offset D8)
SPKR	No Reboot, Rising Edge of PWROK.	Sampled high: this indicates that the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h: bit 5).
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33 / HDA_DOCK_EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK. (Mobile Only)	Sampled low: the Flash Descriptor Security will be overridden. Sampled high: the security measures will be in effect. This strap should only be enabled in manufacturing environments.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be high for mobile applications.
SPI_MOSI (Mobile Only)	Integrated TPM Enable. Rising Edge of CLPWROK.	Sampled low: the Integrated TPM will be disabled. Sampled high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enabled. NOTE: This signal is required to be floating or pulled low for desktop applications.

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRS LPVR / GPIO16	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN# / GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT0#, GNT[3:1]# / GPIO[55, 53, 51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LAD[3:0]# / FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ0	PULL-UP 20K
LDRQ1 / GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1# / GPIO58 (Desktop Only) / CLGPIO6 (Digital Office Only)	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP3	PULL-UP 20K
USB[11:0] [P,N]	PULL-DOWN 15K

PCIE Routing

LANE1	
LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB Pair	Device
0	USB0
1	RESERVED
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Others = Reserved
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	ITPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2). 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 etc. 1 = Normal operation (default): Lane Numbered in Order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG12	ALLZ	0 = ALLZ mode enabled (Note 3) 1 = Disable (Default)
CFG13	XOR	0 = XOR mode enabled (Note 3) 1 = Disable (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIE	0 = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) 1 = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA (Note4)	SDVO Present	0 = No SDVO/HDMI/DP interface disabled (default) 1 = SDVO/HDMI/DP interface enabled
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Note4)	Digital Display Present	0 = Digital display (HDMI/DP) device absent (default) 1 = Digital display (HDMI/DP) Device Present
CFG4:3 CFG8 CFG11 CFG14 CFG15 CFG17 CFG18	Reserved	

NOTE:

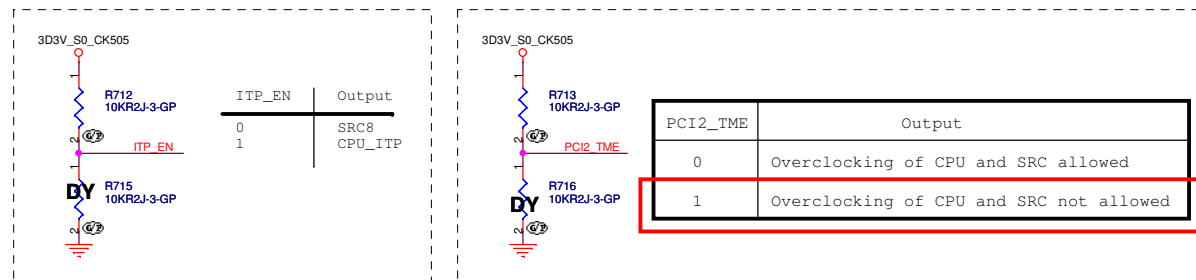
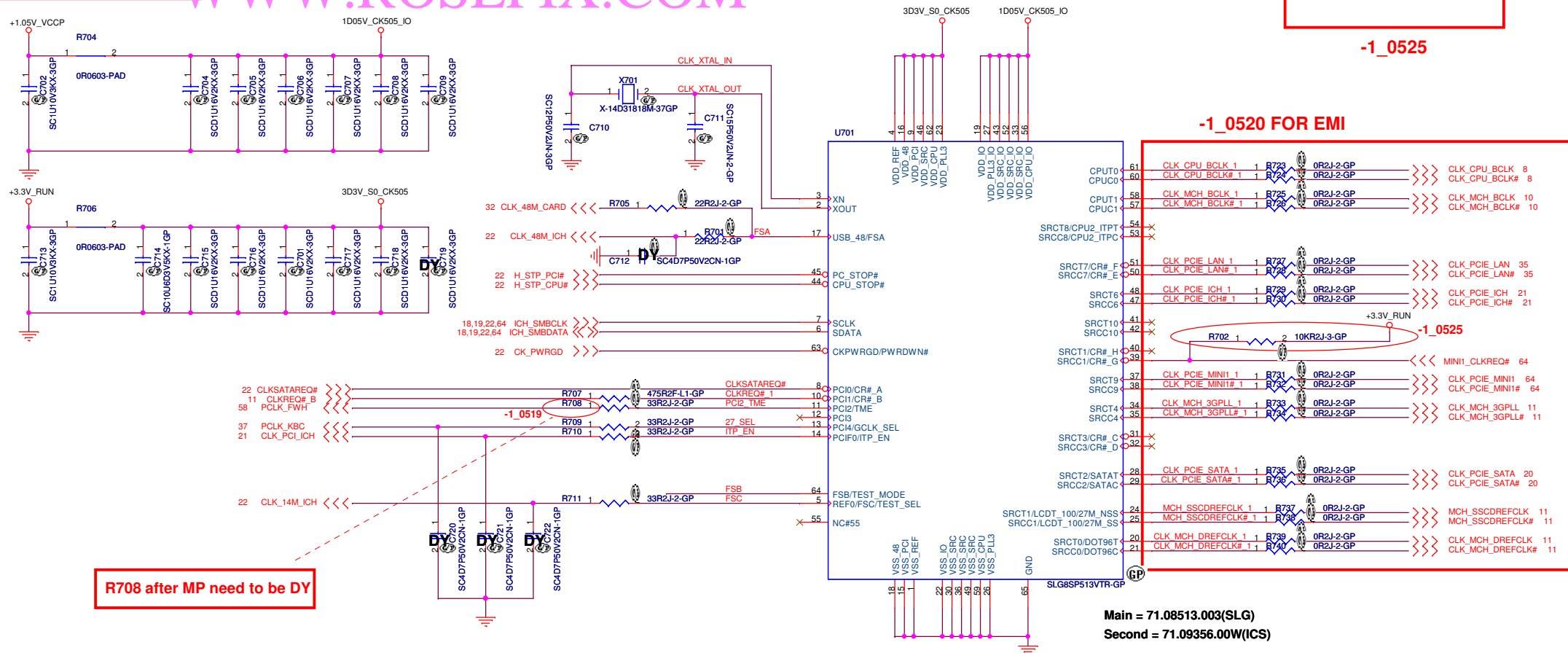
- All strap signals are sampled with respect to the leading edge of the GMCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.
- DDPC_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable Display Port.

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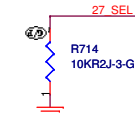
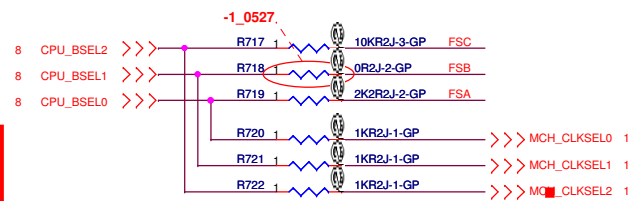
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SSID = CLOC

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SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M



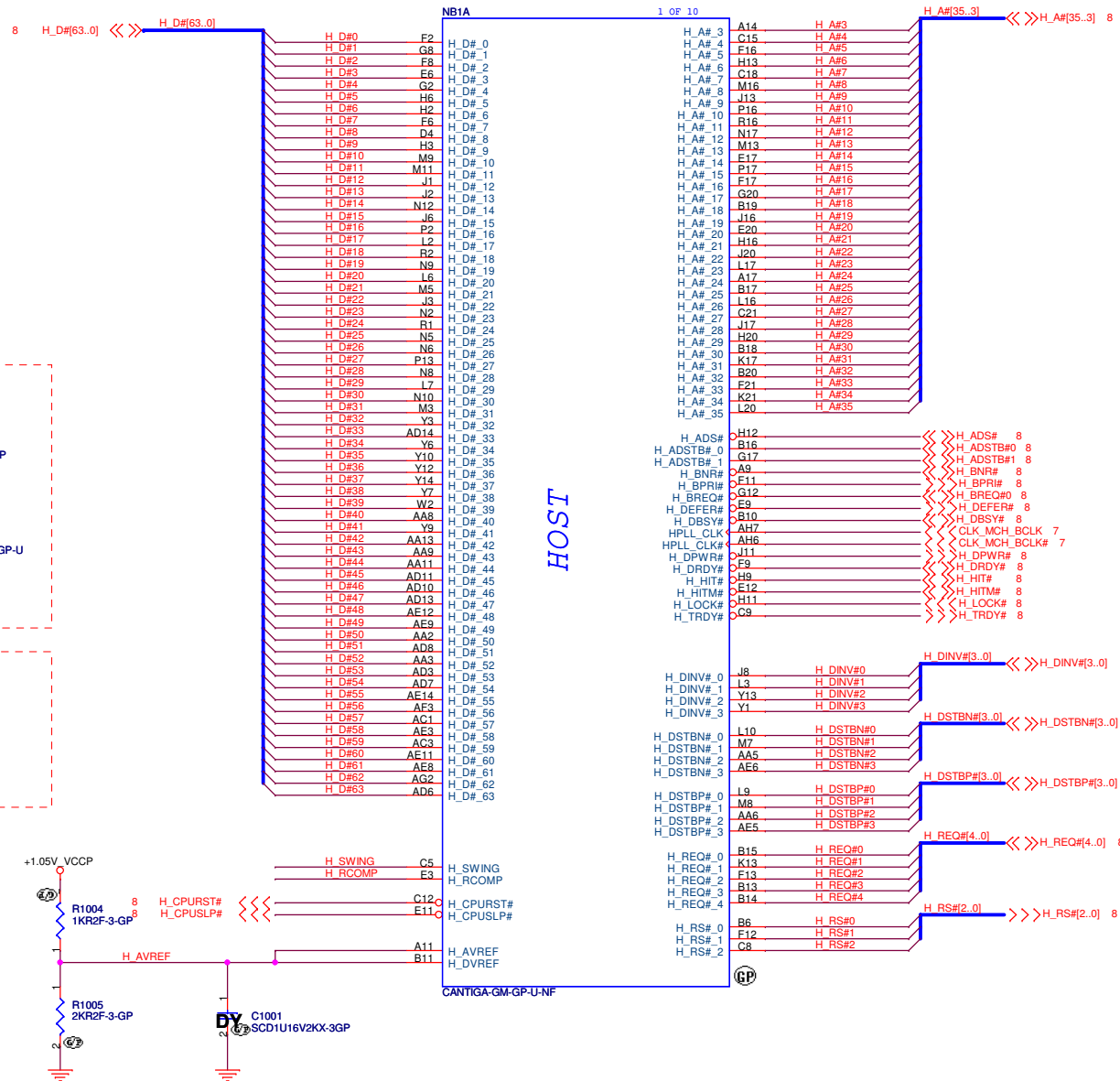
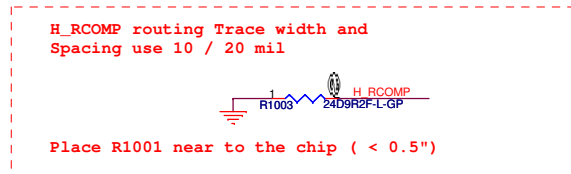
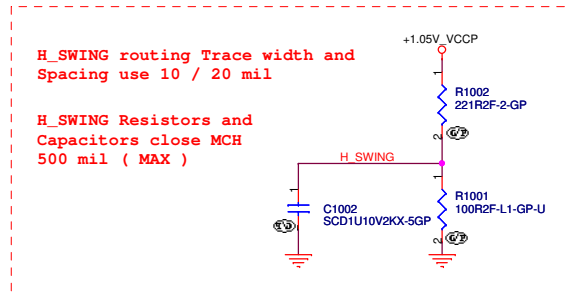
27_SEL	PIN20/21	PIN24/25
0	96M	100M
1	100M	27M

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SSID = MCH

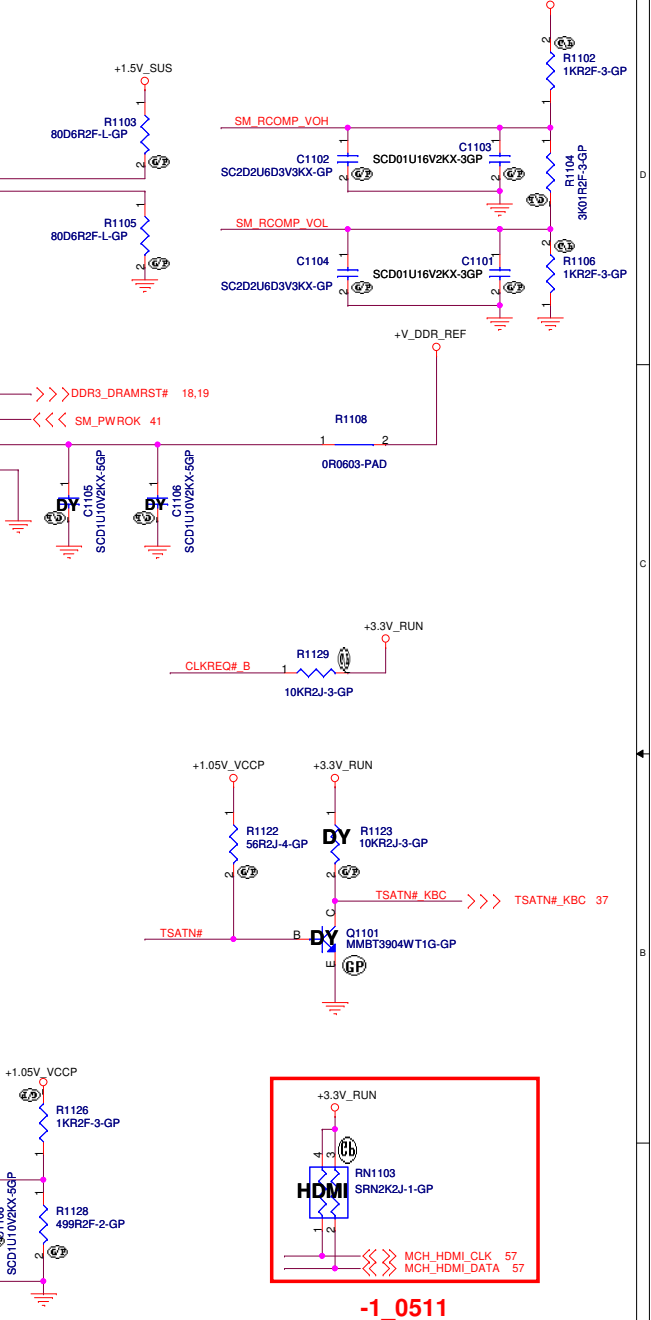
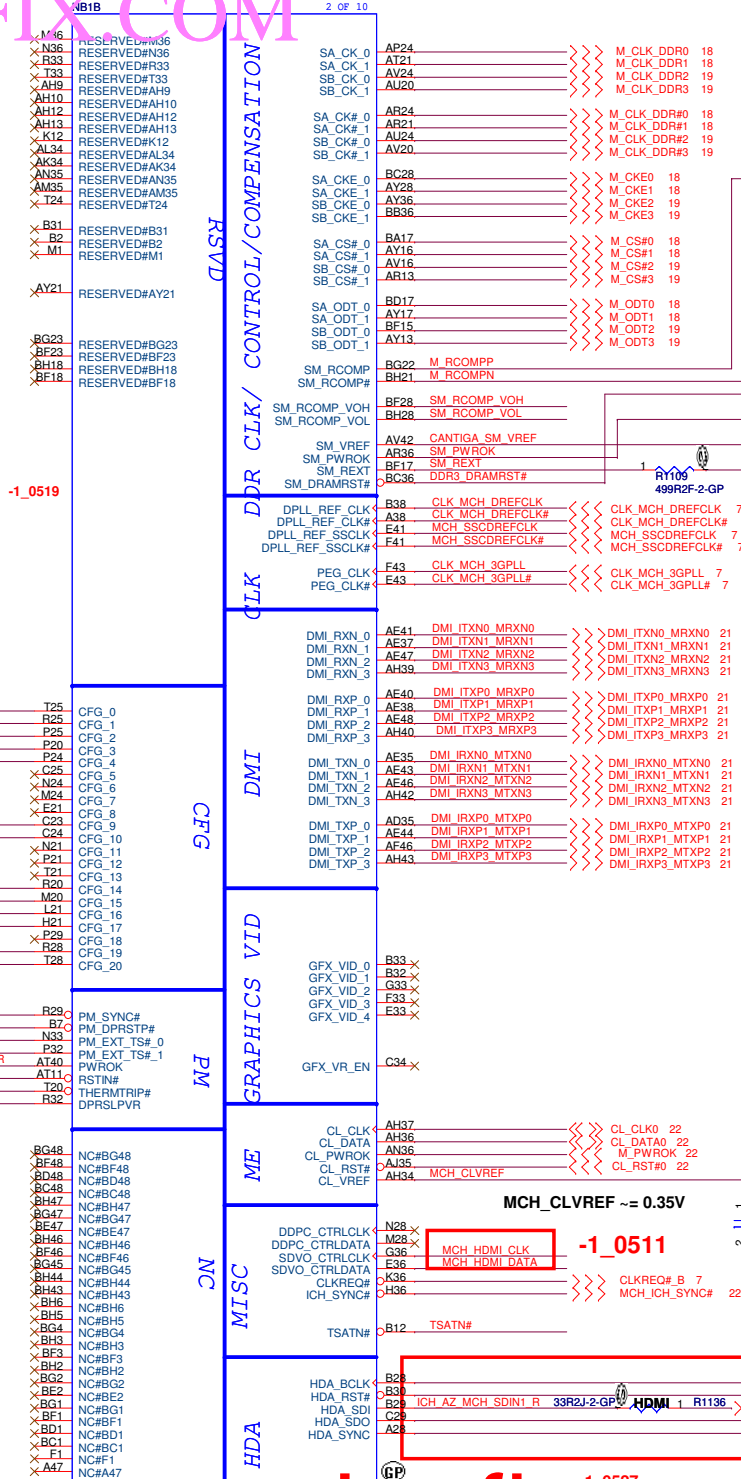
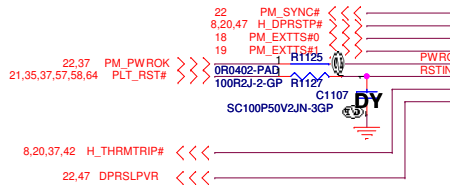
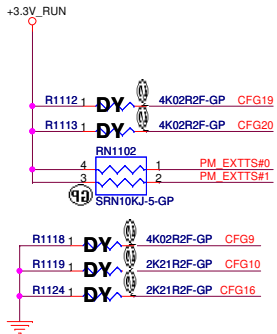
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SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in order *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19	Normal operation	Reverse DMI lanes *
CFG 20	SDVO concurrent with PCIE	PCIE and SDVO are operating simultaneously via the PEG port *
SDVO_CTRLDATA	SDVO interface disable	SDVO interface enable (HDMI enable) *
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled



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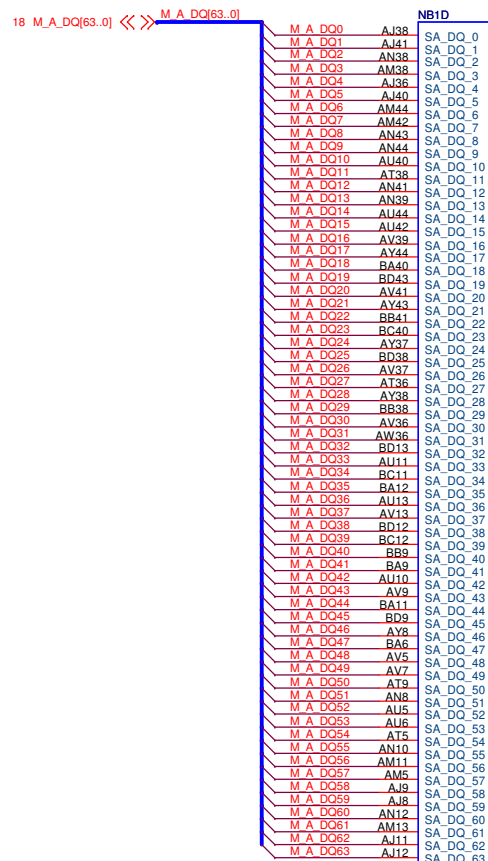
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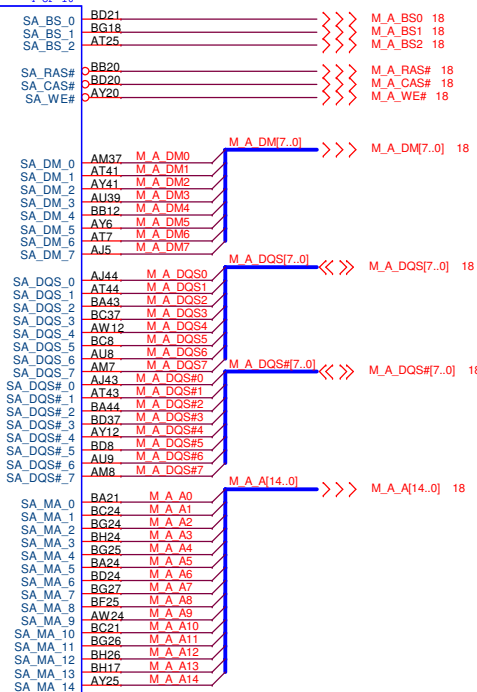
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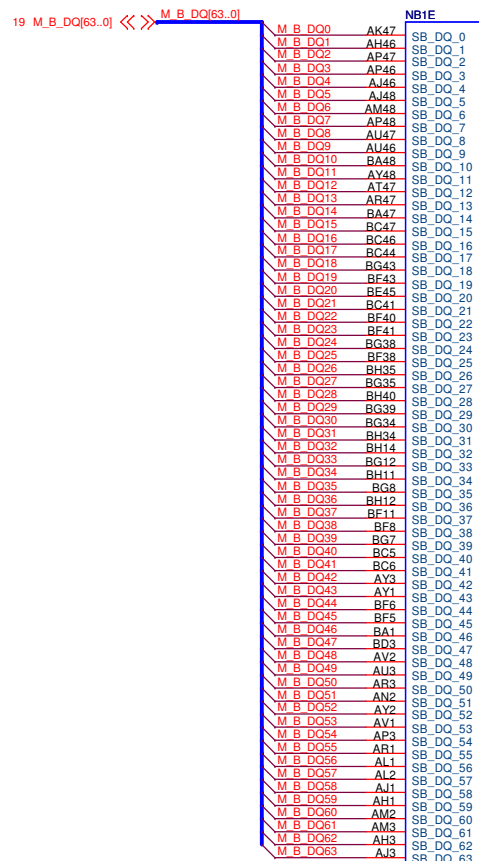
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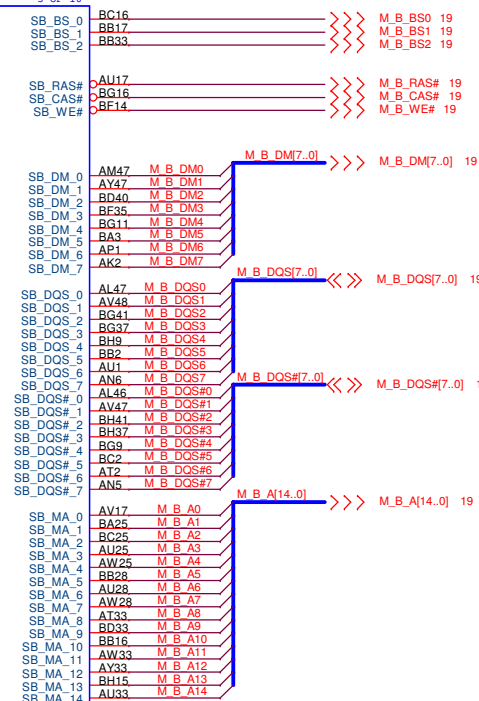
DDR SYSTEM MEMORY A



CANTIGA-GM-GP-U-NF



DDR SYSTEM MEMORY B



CANTIGA-GM-GP-U-NF

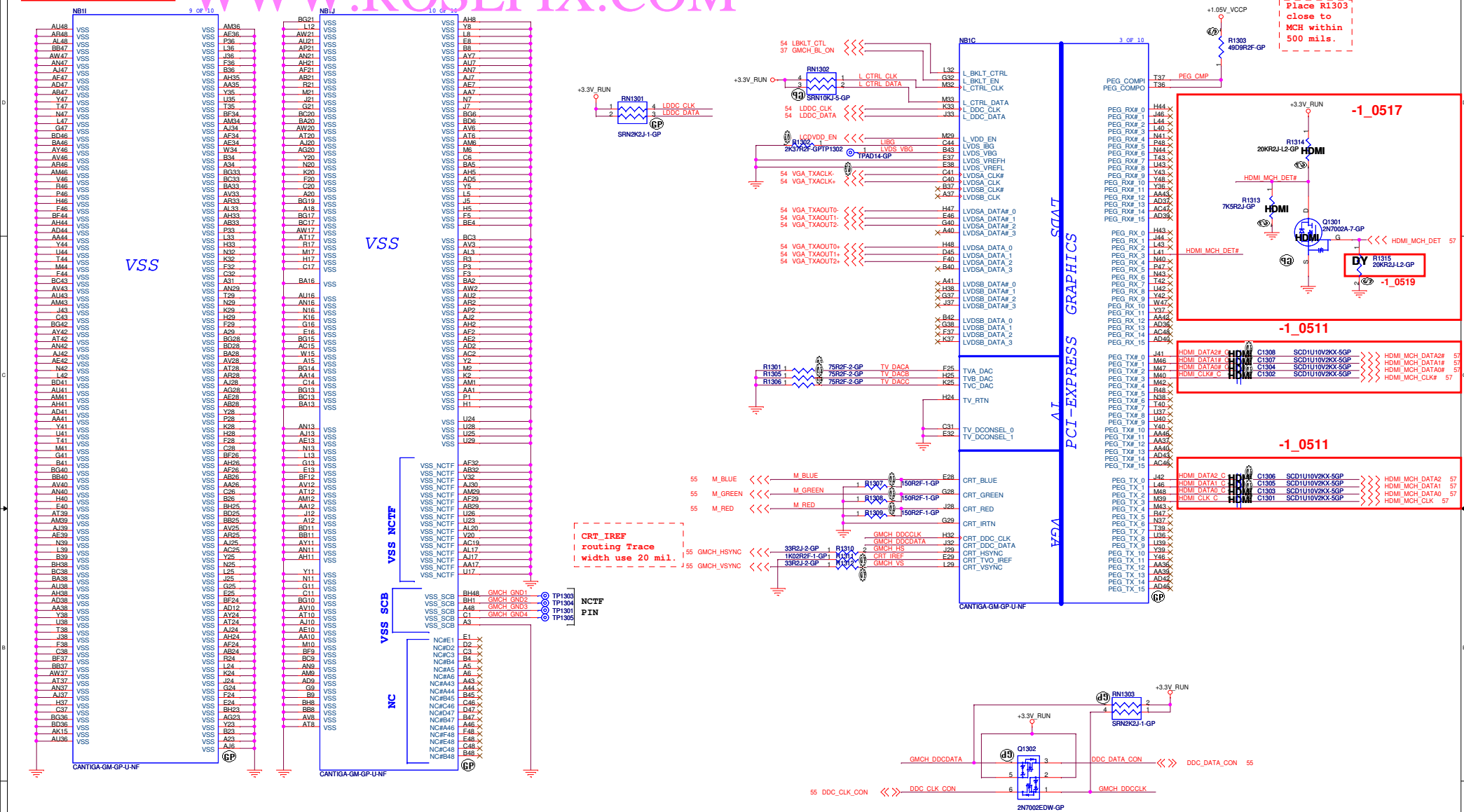
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SSID = MCH

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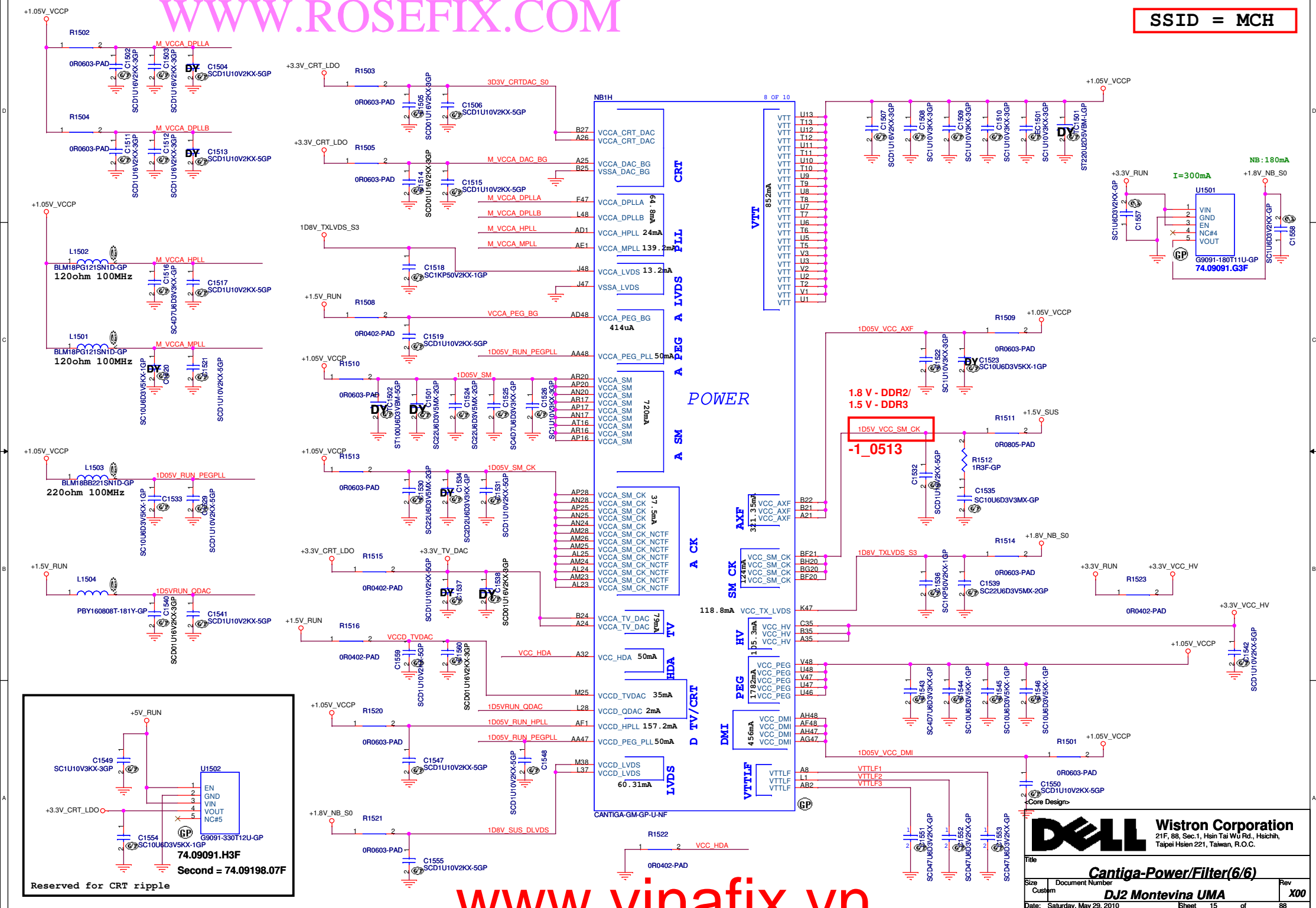
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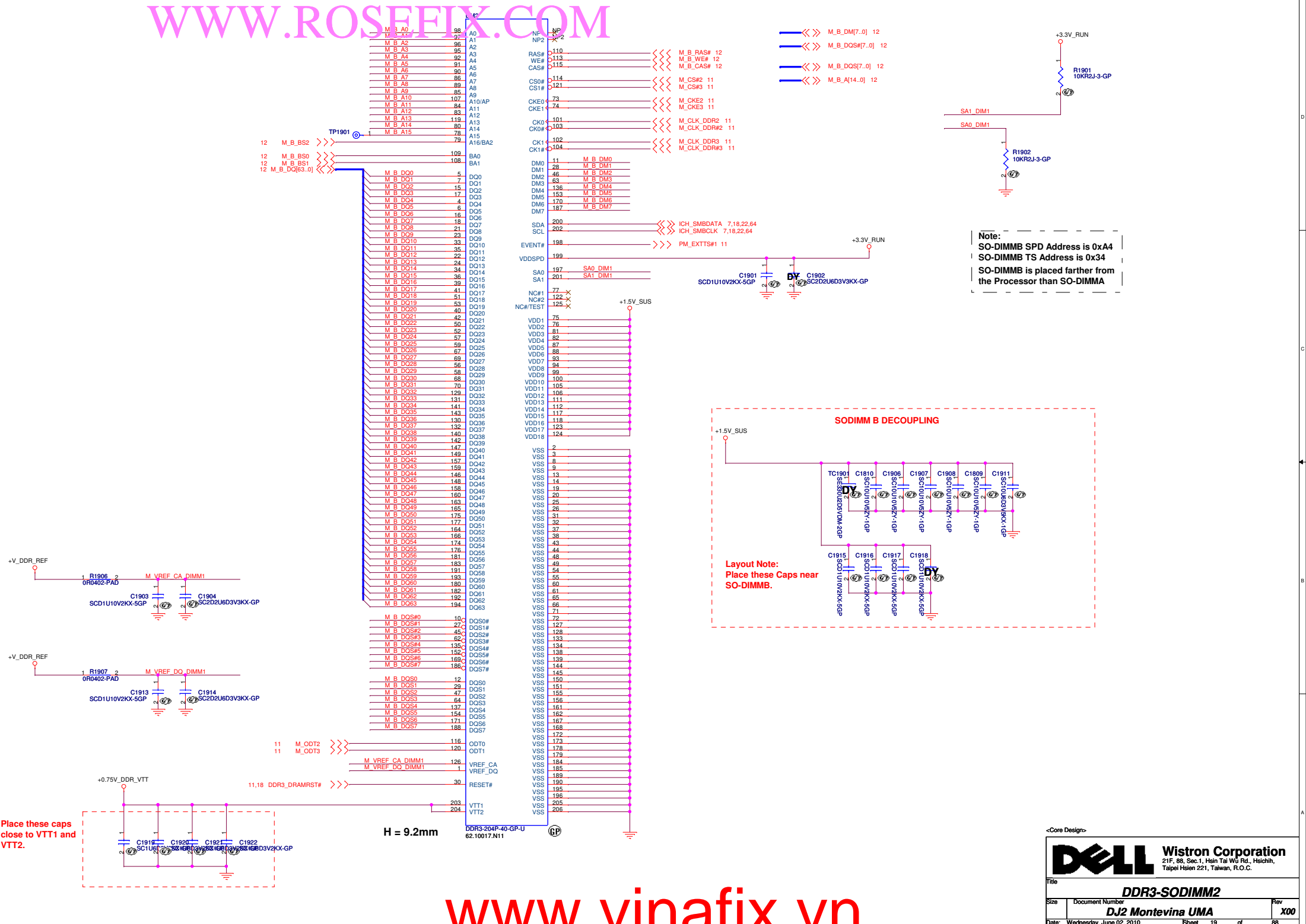
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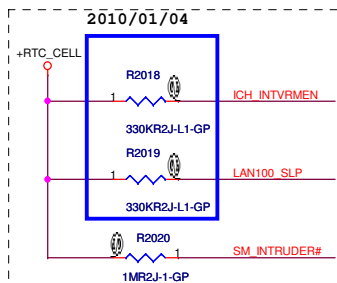
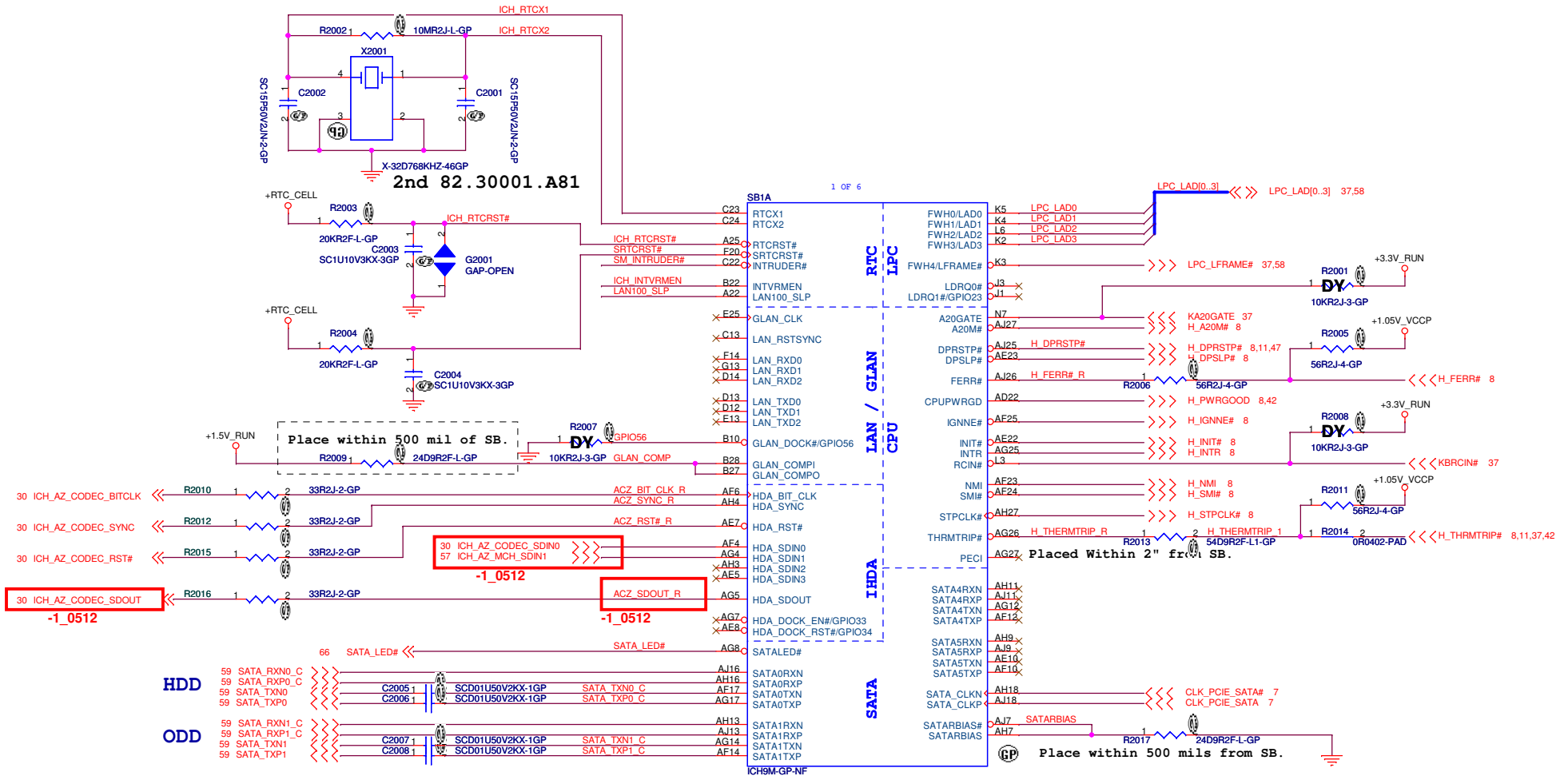
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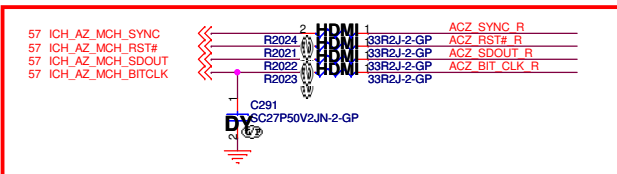
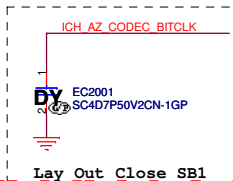


SSID = ICH

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integrated VccSus1_05,VccSus1_5,VccCLI_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCLI_05	
LAN100_SLP	High=Enable Low=Disable



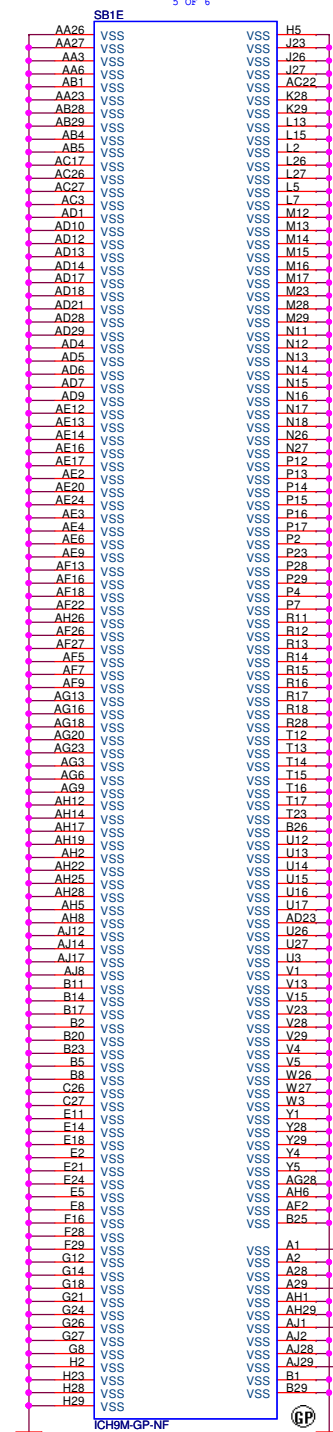
-1_0512
HDA level shift for HDMI

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Title ICH9-LAN/HDA/SATA/LPC(1/4)			
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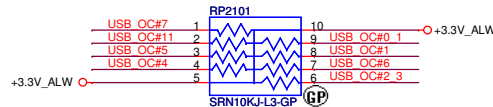
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SSID = ICH



11,35,37,57,58,64 PLT_RST# <<< PLT_RST# R2102 1 2 0R0402-PAD PCI_PLTRST#

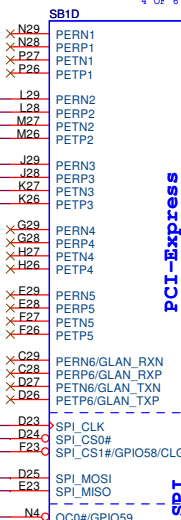
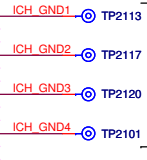
Layout Note:
Place as close as possible
to the ICH Pin



WLAN

LAN

NCTF PIN



PCI-Express

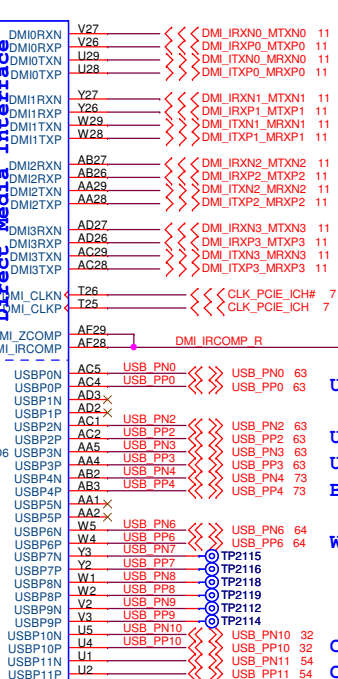
SPI

USB

WLAN

Card Reader

CAMERA



PCI-Express

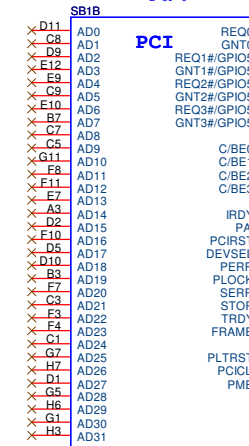
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USB

WLAN

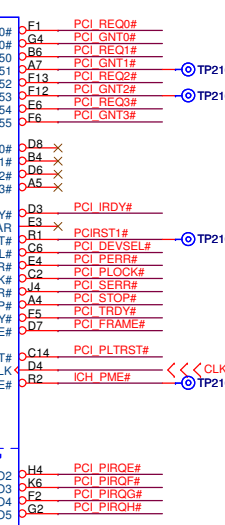
Card Reader

CAMERA



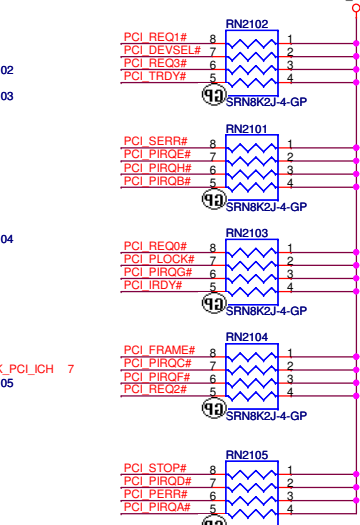
PCI

Interrupt I/F



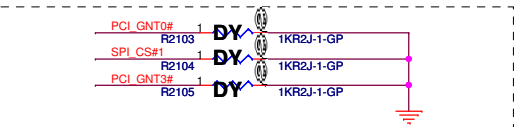
PCI

Interrupt I/F



PCI

Interrupt I/F

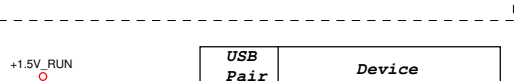


PCI

Interrupt I/F

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)

A16 swap override strap
low = A16 swap override enable
high = default

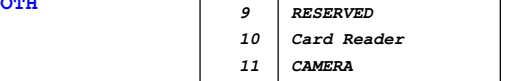


PCI

Interrupt I/F

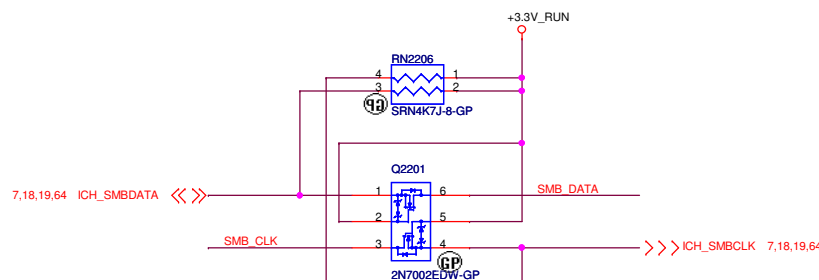
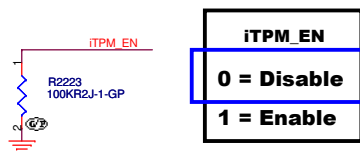
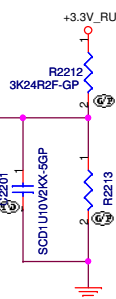
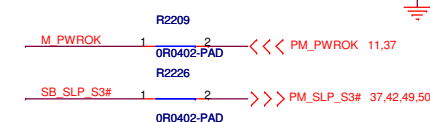
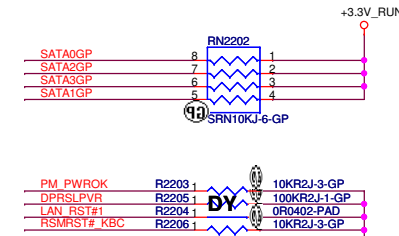
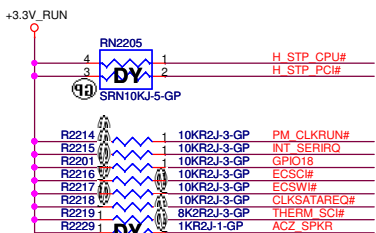
USB Pair	Device
0	USB0
1	RESERVED
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Core Design

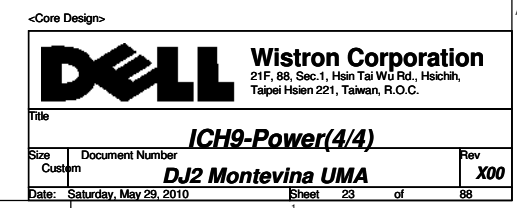
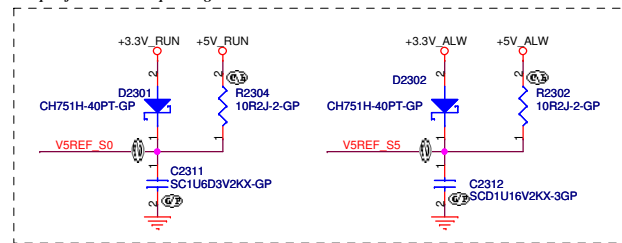


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ICH9-PCI/PCIE/DMI/USB/GND(2/4)
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 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
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Size Custom	Document Number DJ2 Montevina UMA	Rev X00
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<Core Design>



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Size
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Title			
Reserved			
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<Core Design>



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Title

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Size
A3

Document Number

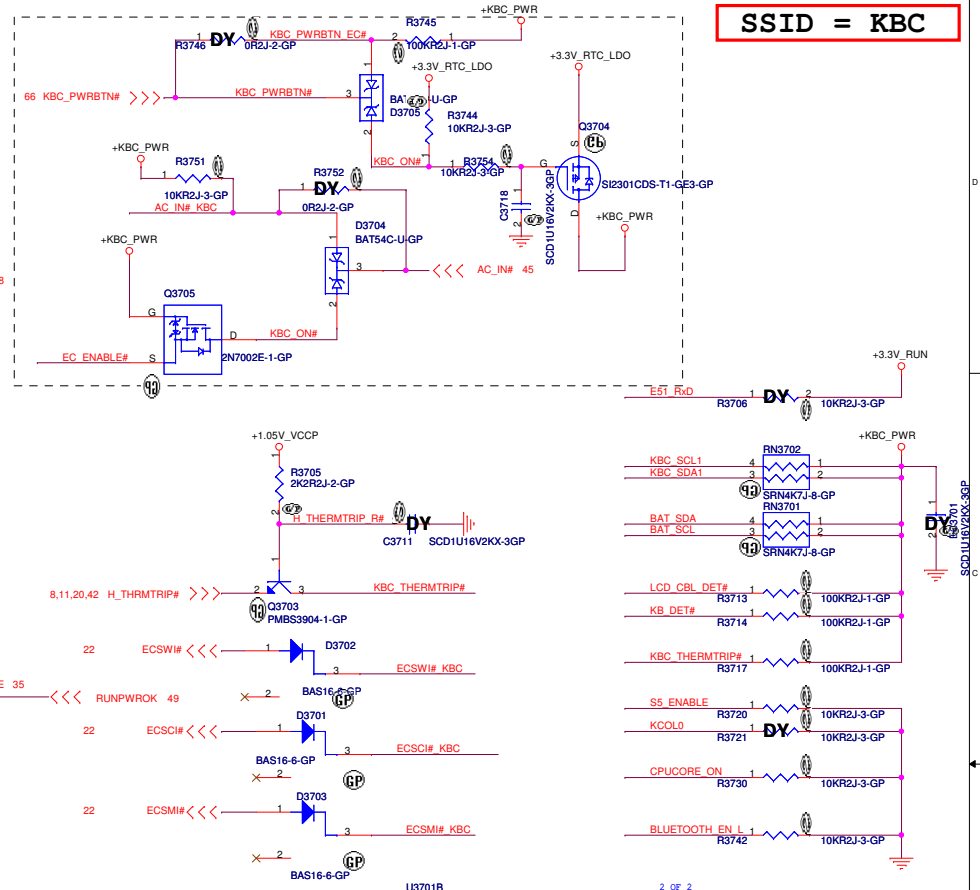
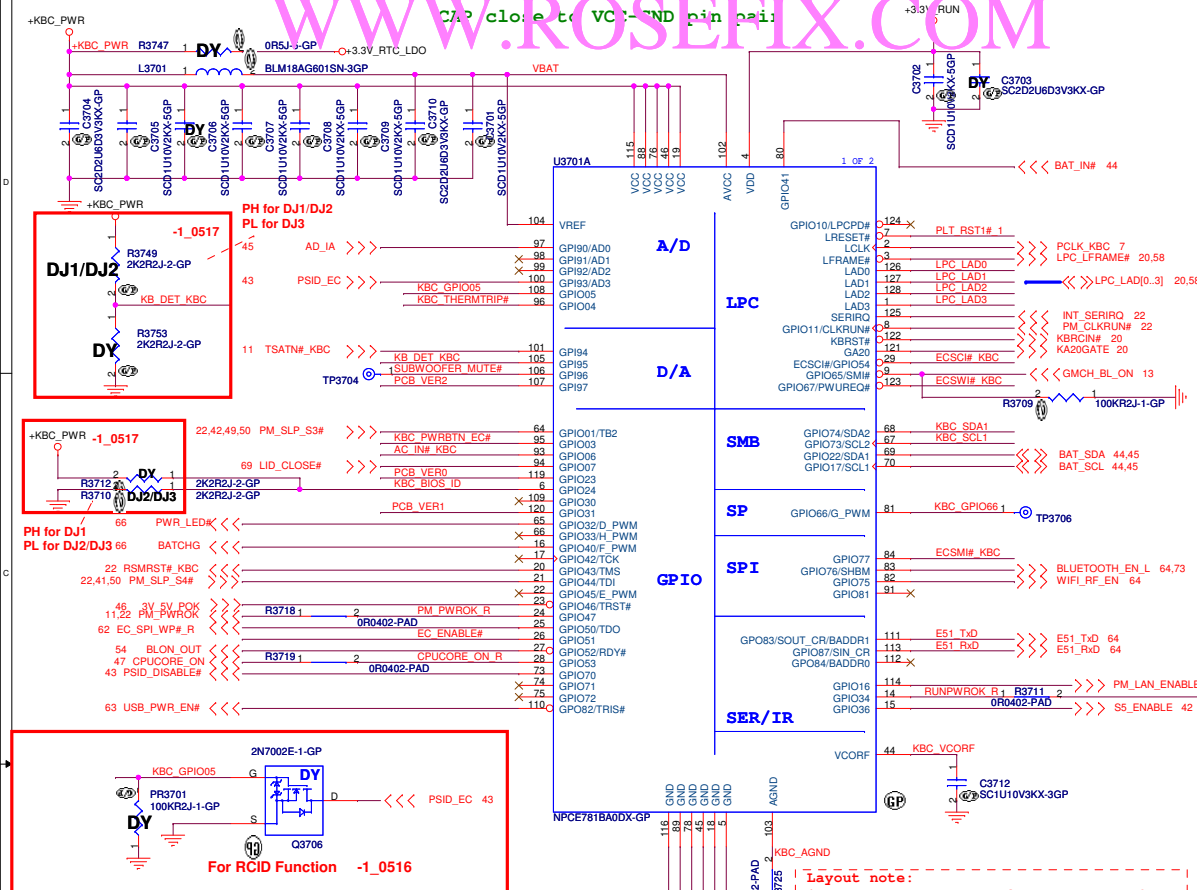
DJ2 Montevina UMA

Rev

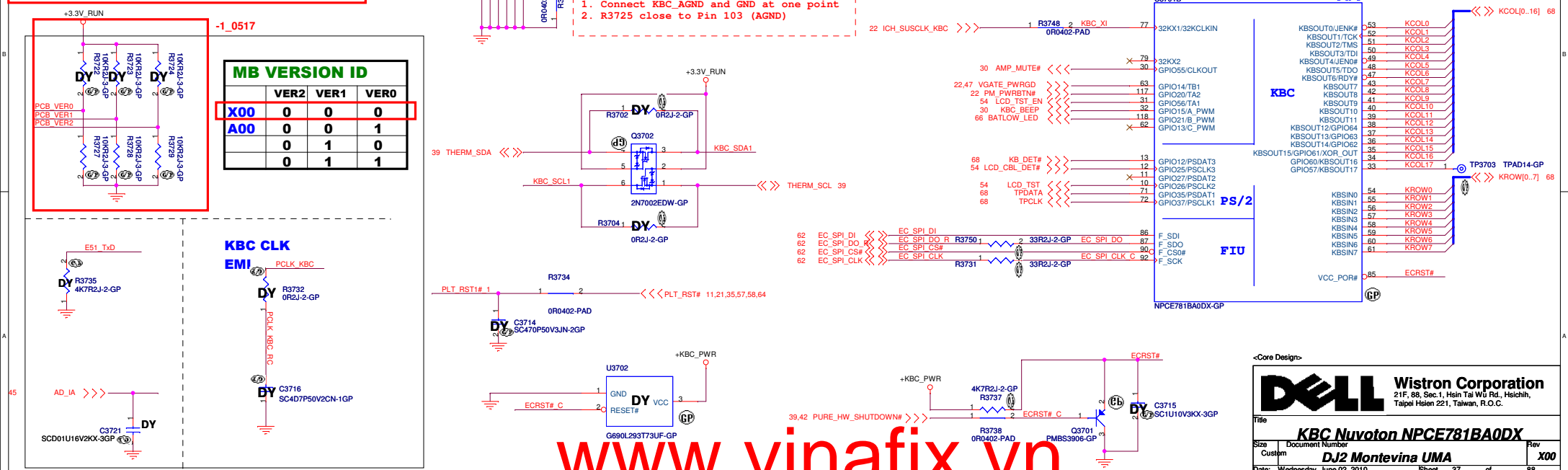
X00

Date: Friday, May 28, 2010

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MB VERSION ID			
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X00	0	0	0
A00	0	0	1
	0	1	0
	0	1	1



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Title

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Size
A3

Document Number

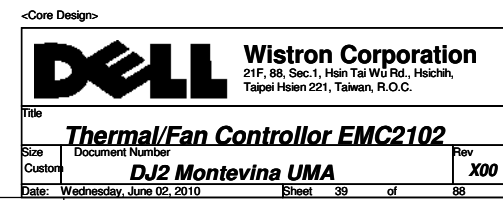
DJ2 Montevina UMA

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<Core Design>



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Title

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A3

Document Number

DJ2 Montevina UMA

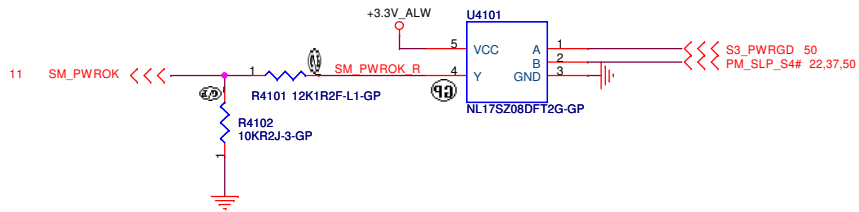
Rev

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SSID = Reset.Suspend



<Core Design>



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Title

Power On Logic

Size
A3

Document Number

DJ2 Montevina UMA

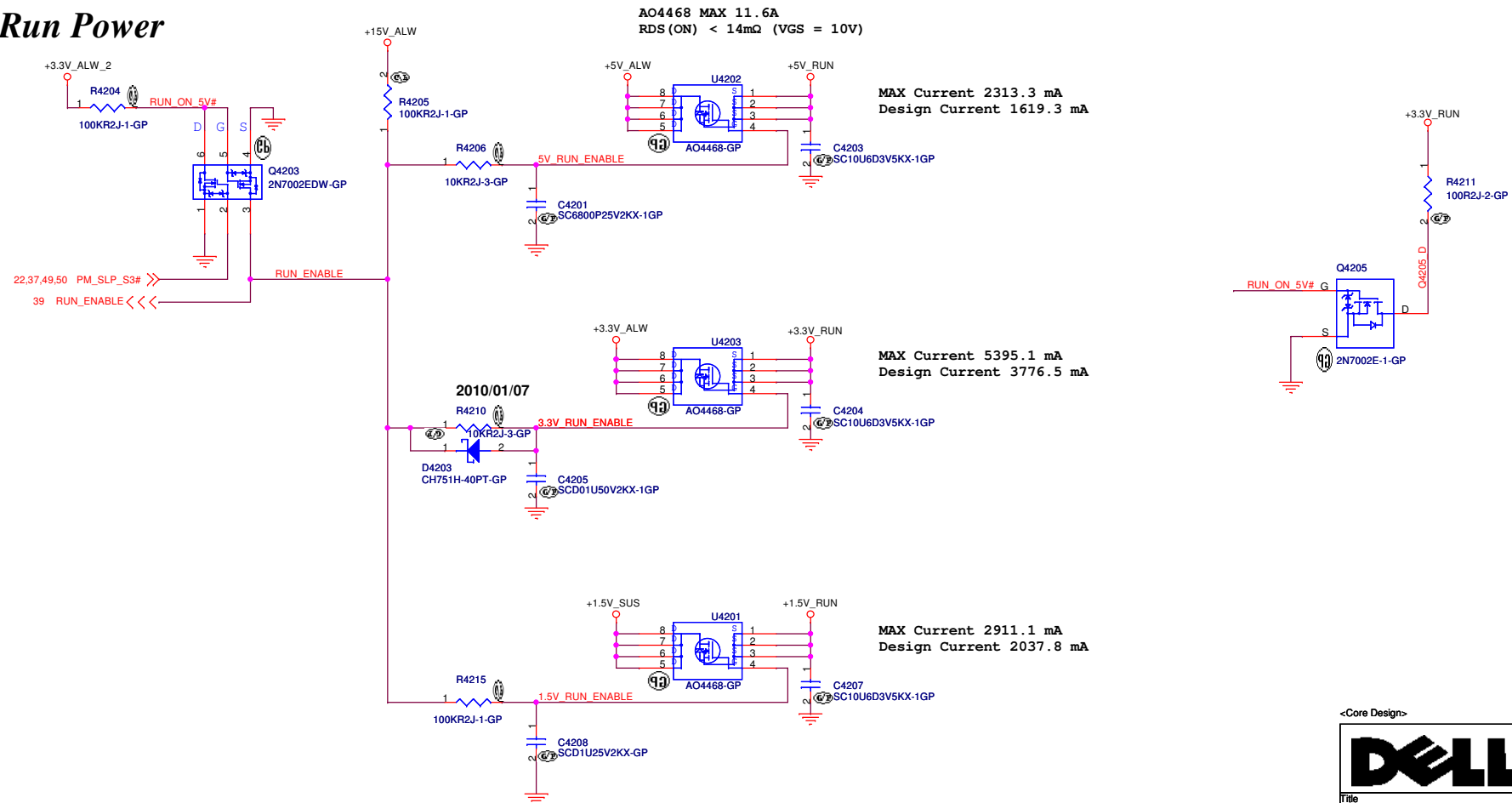
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Run Power



<Core Design>



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Title

Power Plane Enable

Size
A3

Document Number	
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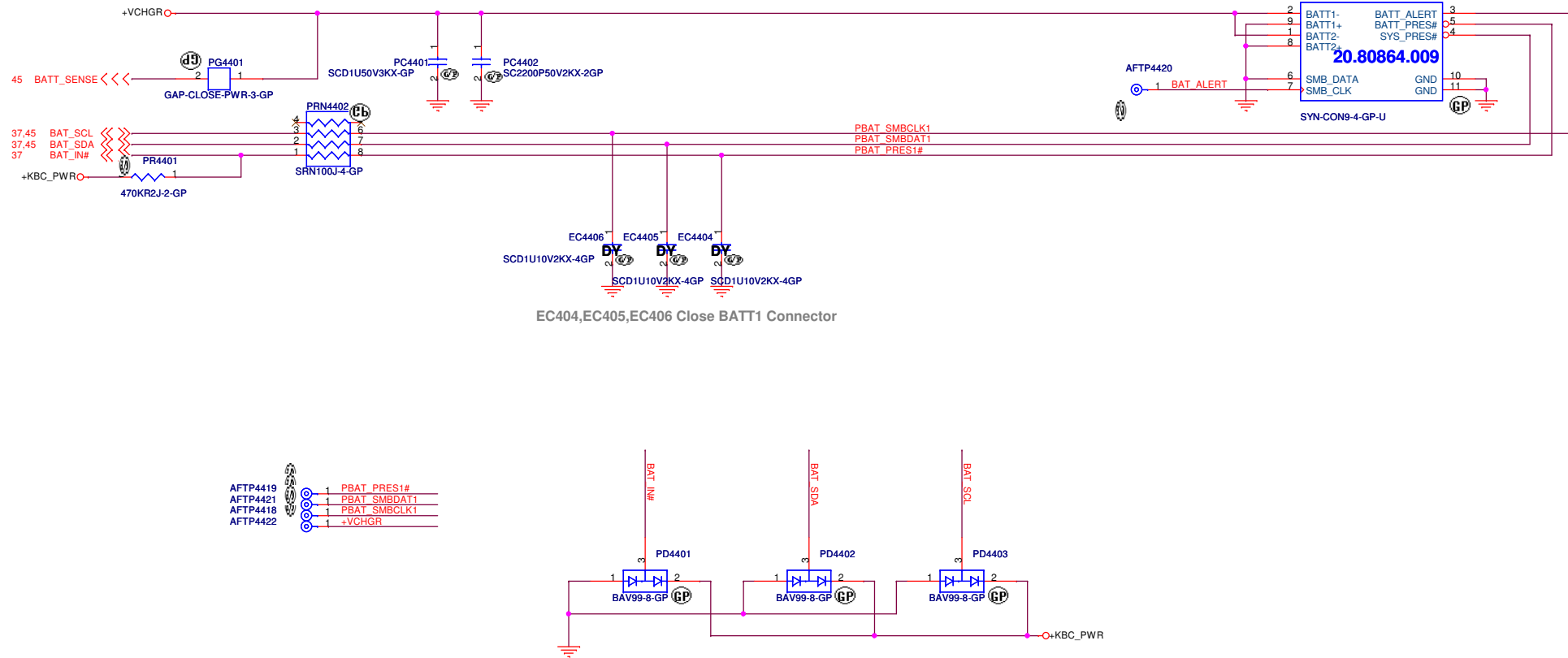
DJ2 Montevina UMA

Rev

Date: Wednesday, June 02, 2010

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Batt Connector



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Title

BATT CONN

Size

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Rev

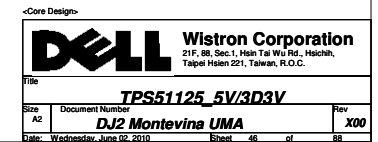
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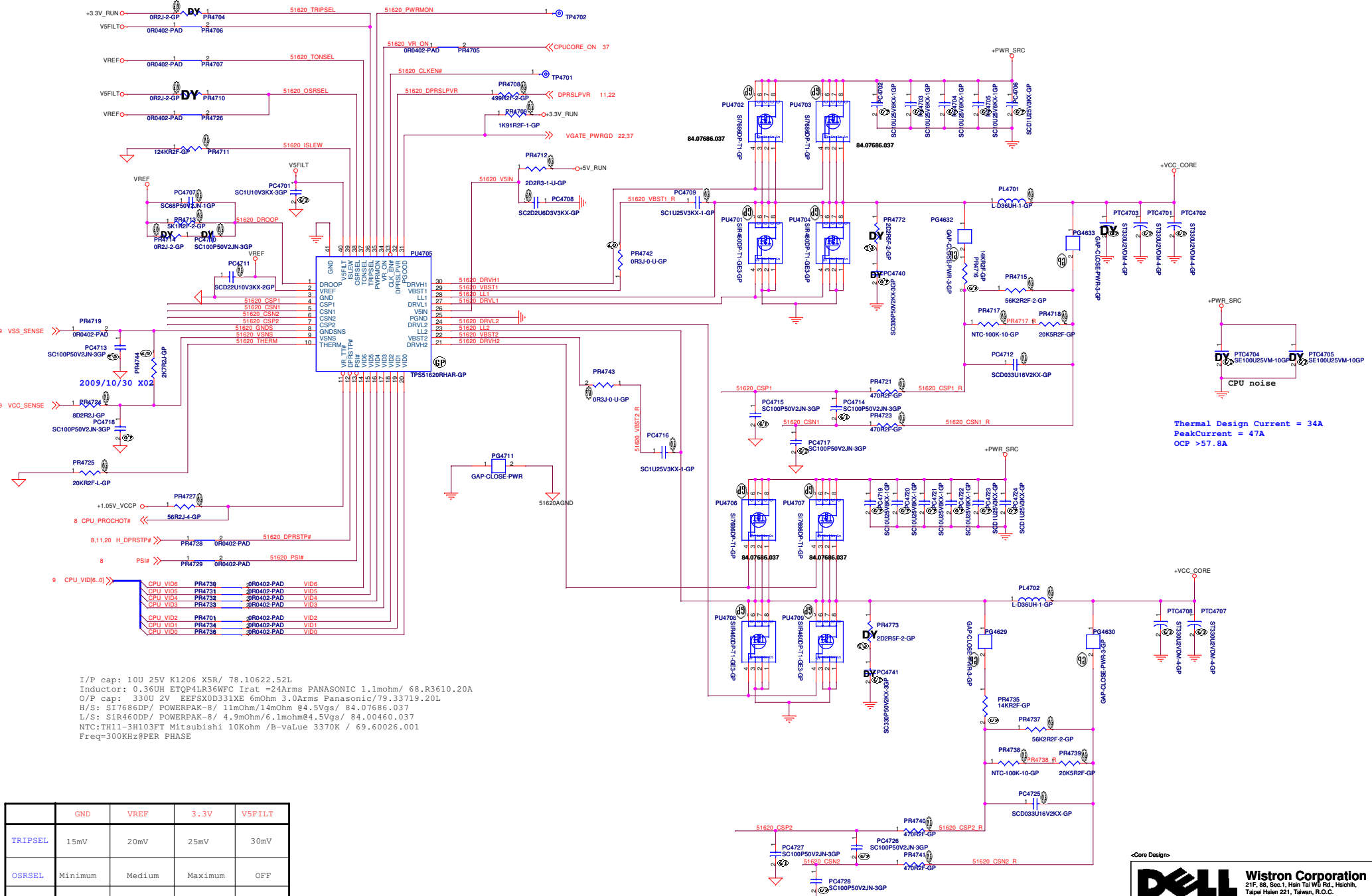
Date: Wednesday, June 02, 2010

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	GND	VREF	3.3V	V5FILT
TRIPSEL	15mV	20mV	25mV	30mV
OSRSEL	Minimum	Medium	Maximum	OFF
TONSEL	200KHz	300KHz	400KHz	500KHz
OVFSEL	ENABLE	DISABLE	N/A	N/A

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<Core Design>



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Title

CPU VCORE POWER(2/2)

Size
A3

Document Number

DJ2 Montevina UMA

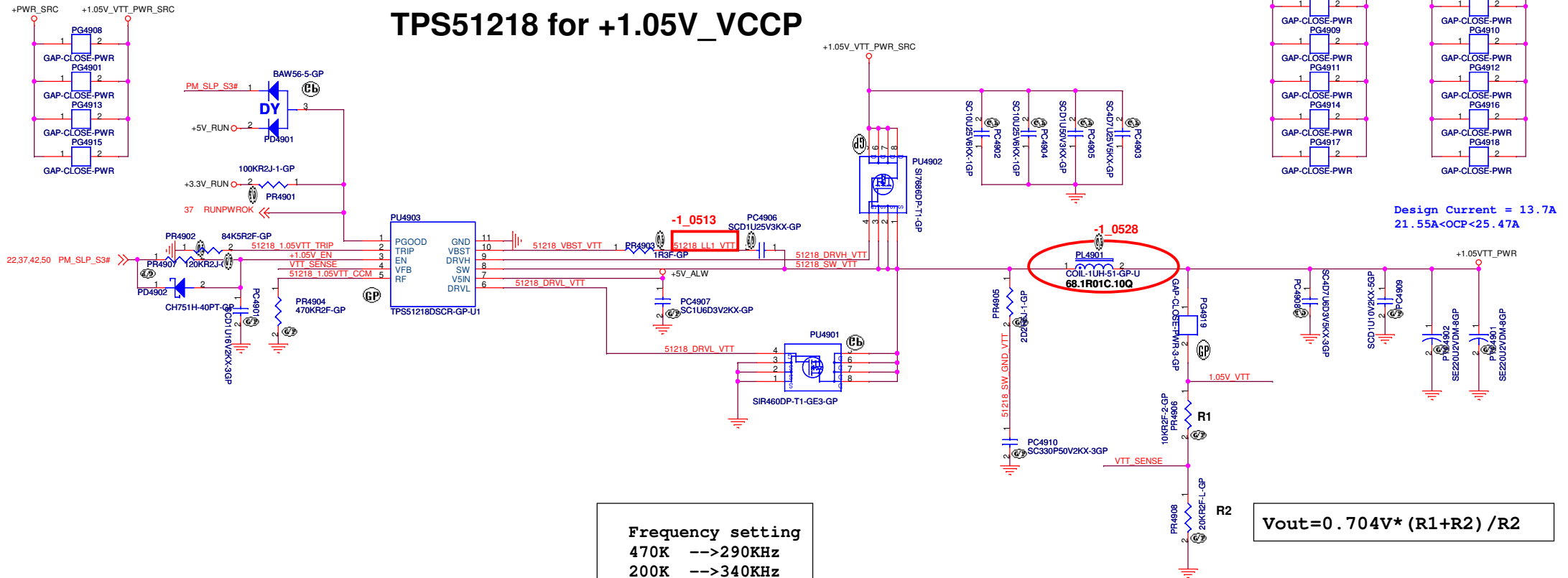
Rev
X00

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SSID = PWR.Plane.Regulator_ip05v

TPS51218 for +1.05V_VCCP

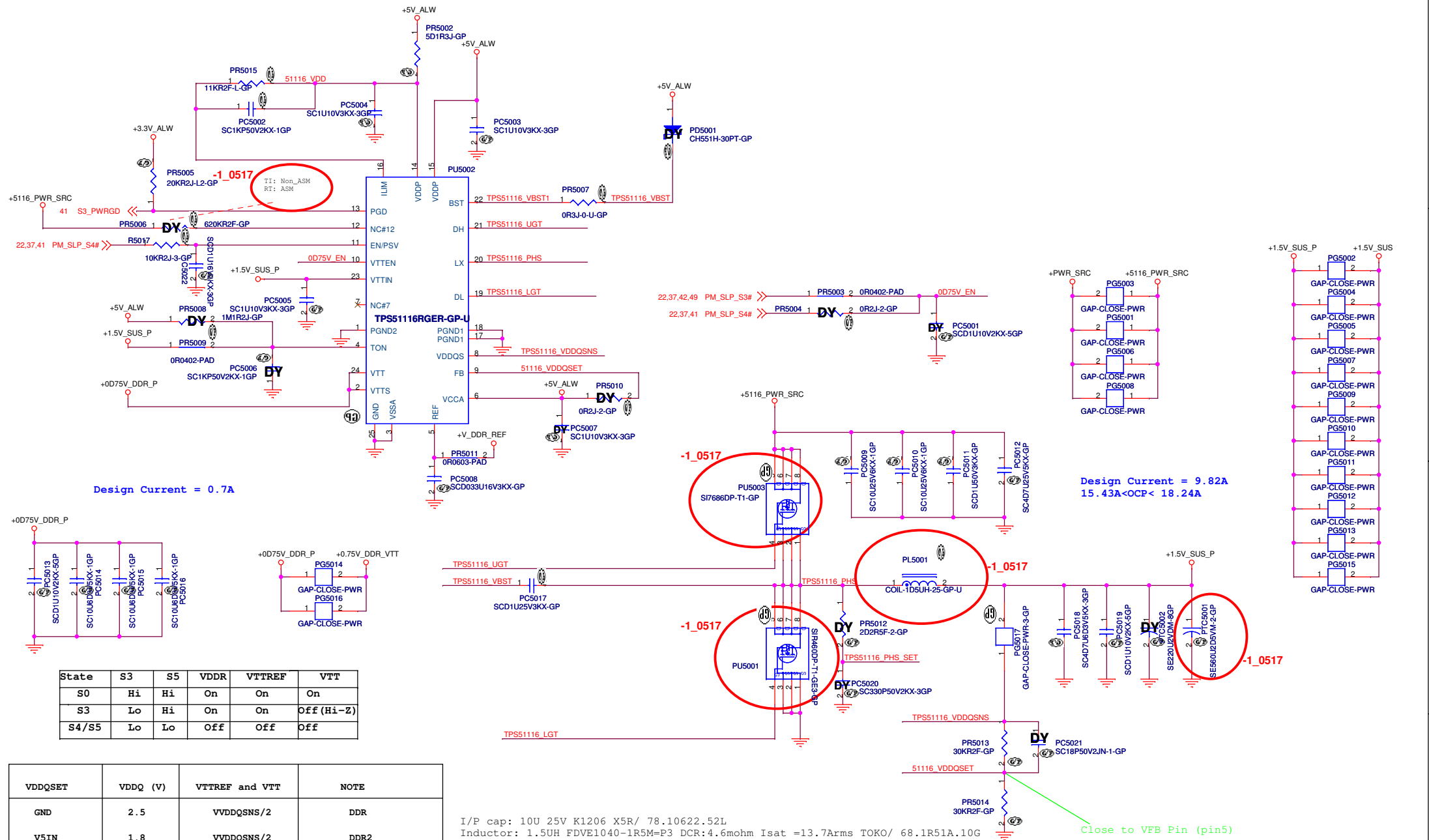


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1uH FDUE1040D-1R0M=P3 TOKO DCR:2.35mohm Isat =17.9Arms 68.1R01B.10A
O/P cap: 220U 2V EEFCX0D221R 15mohm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP-T1-E3/11mohm/ 14mOhm@4.5Vgs/ 84.07686.037
L/S: SIR460DP-T1-GE3-GP/4.5mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

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Title TPS51218 +1.05V VCCP			
Size Custom	Document Number DJ2 Montevina UMA	Rev X00	
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SSID = PWR.Plane.Regulator.1p5V.0p75V



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Title: **TPS51116 +1.5V SUS**

Size: Custom Document Number: **DJ2 Montevina UMA** Rev: **X00**

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

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Reserved			
Size A3	Document Number DJ2 Montevina UMA		Rev X00
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

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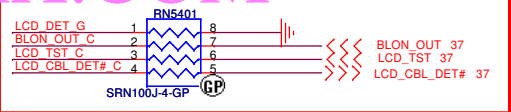
Date: Friday, May 28, 2010

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SSID = VIDEO

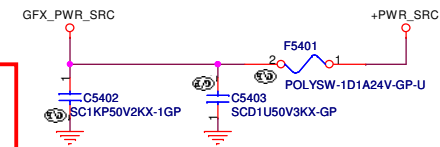
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SSID = Inverter



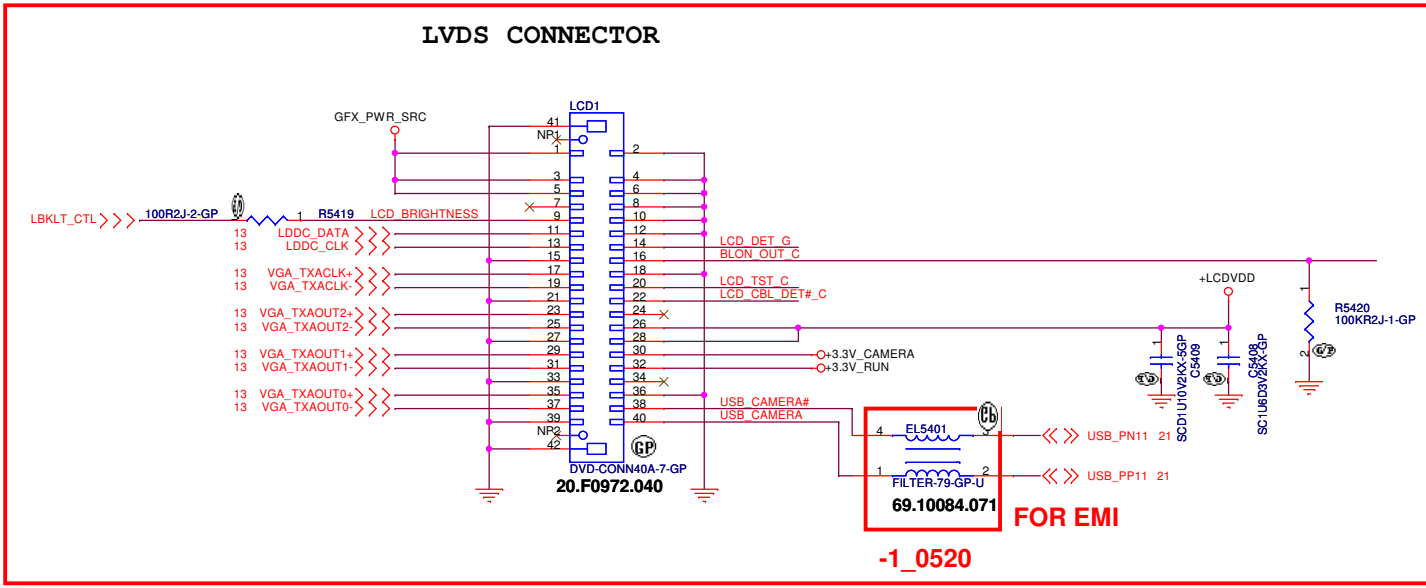
-1_0526
SWAP for Layout

INVERTER POWER

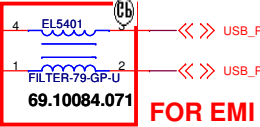


SSID = VIDEO

LVDS CONNECTOR



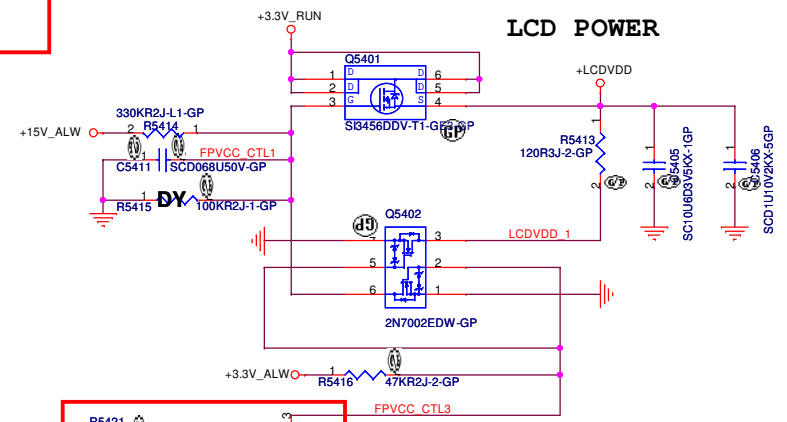
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FOR EMI

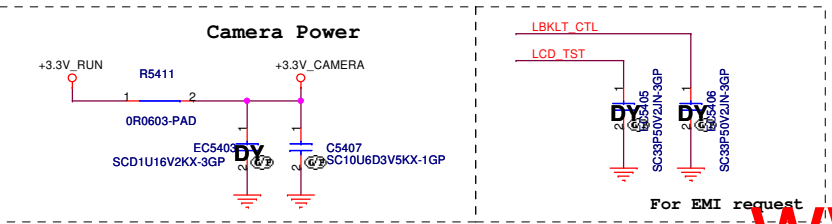
-1_0520

LCD POWER




-1_0525

Camera Power



For EMI request

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Title LCD/Inverter Connector		
Size A3	Document Number DJ2 Montevina UMA	Rev X00
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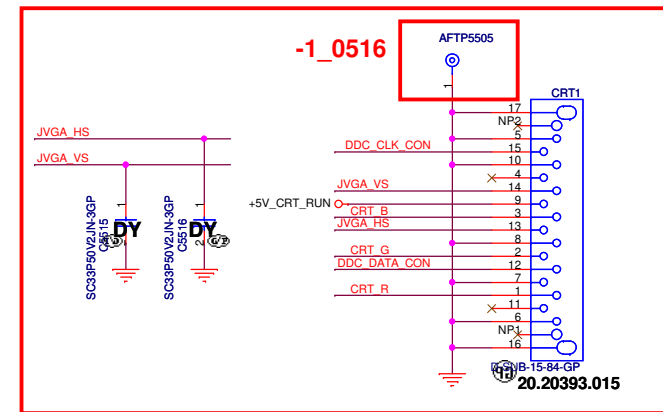
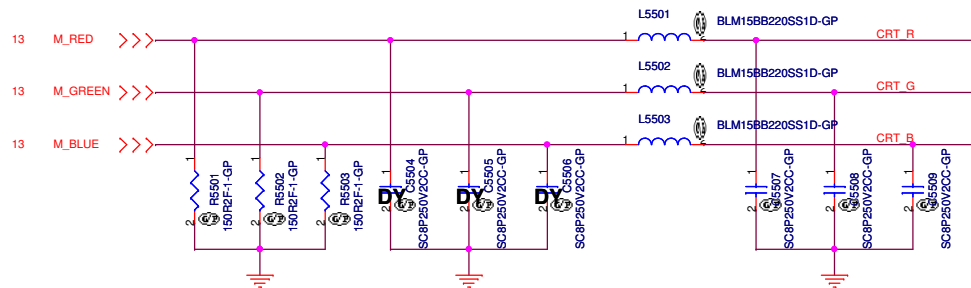
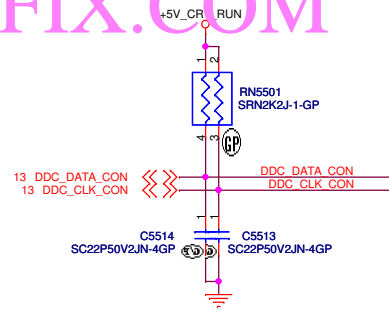
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SSID = VIDEO

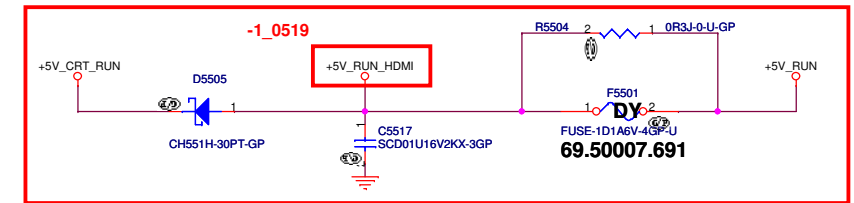
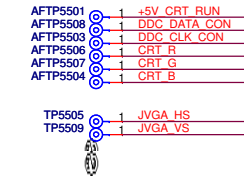
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Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

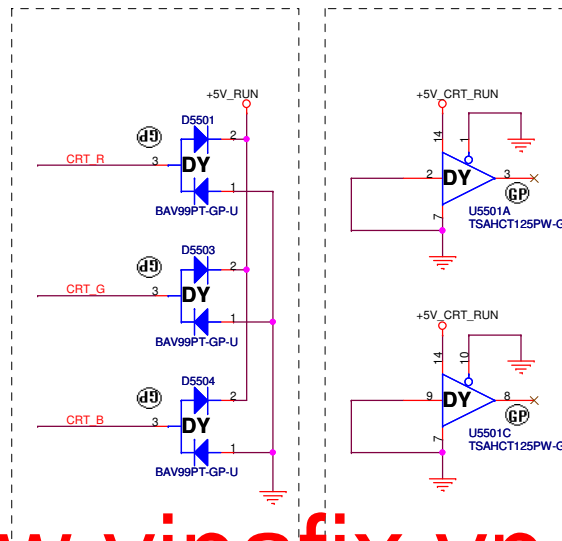
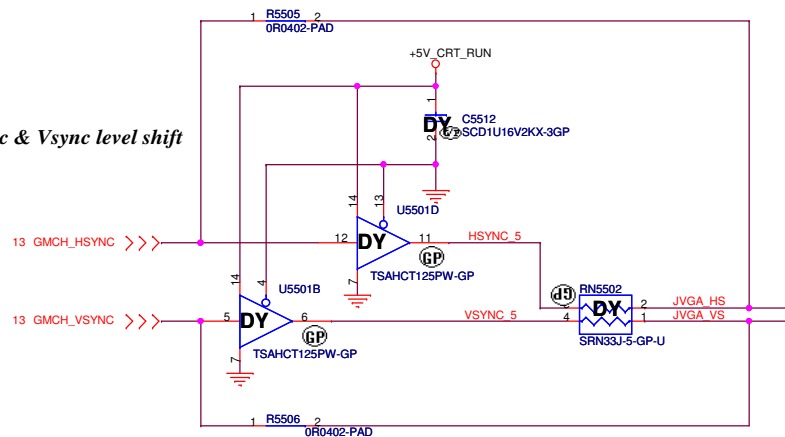


-1_0511



-1_0511 for safety option

Hsync & Vsync level shift



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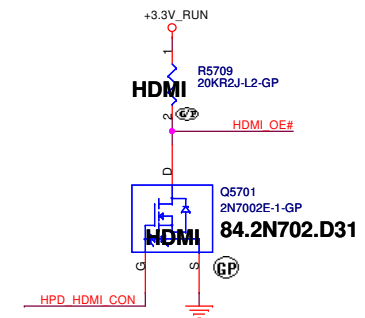
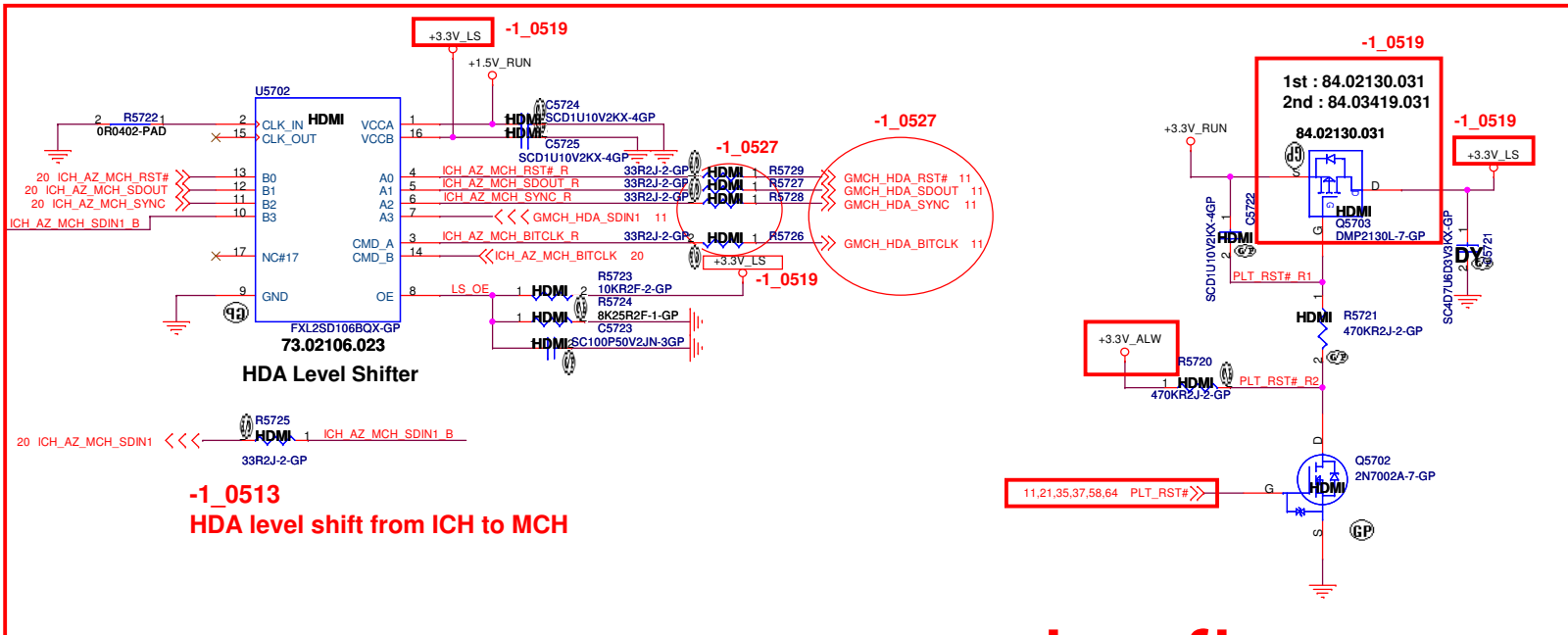
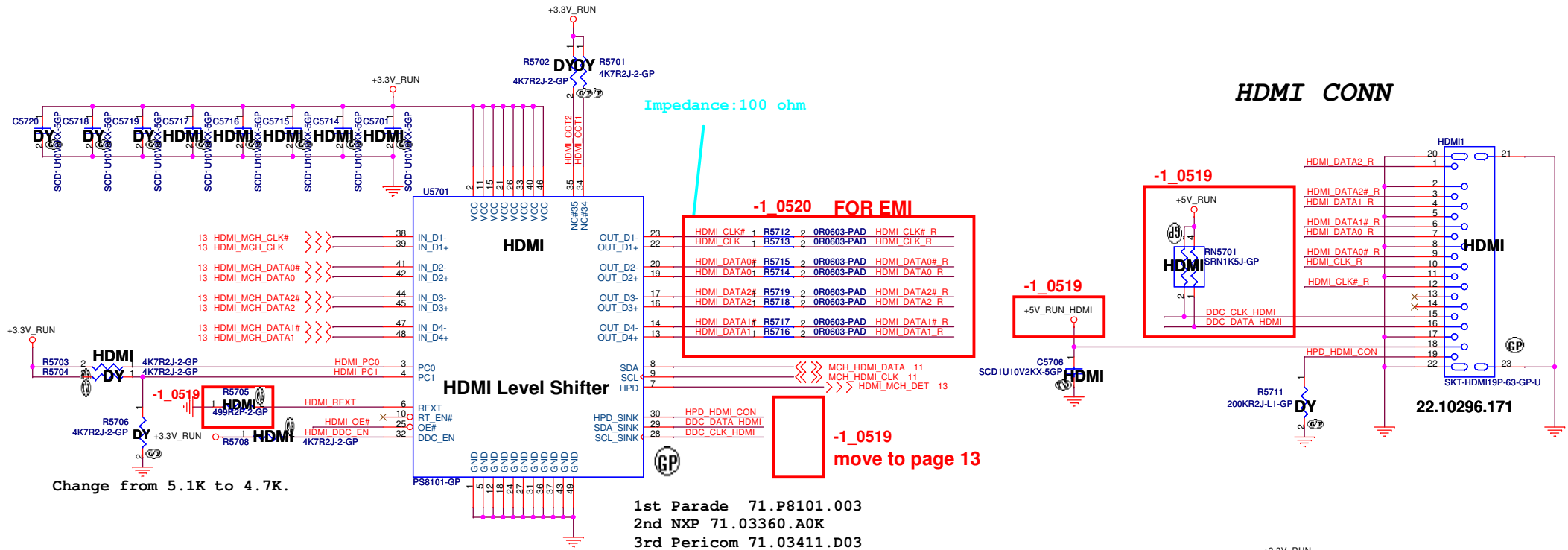
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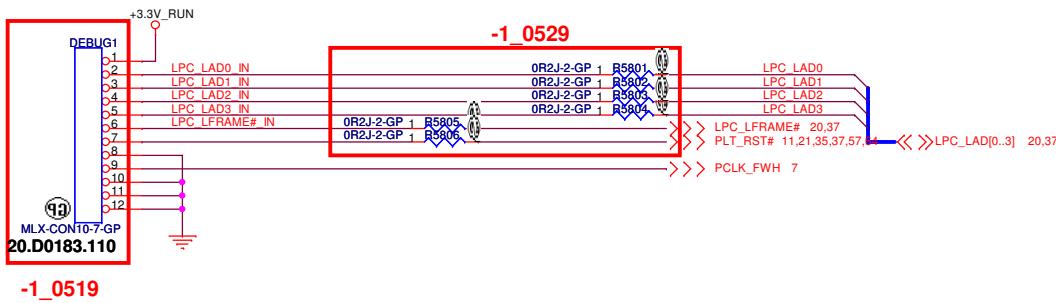
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Title			
Reserved			
Size A3	Document Number DJ2 Montevina UMA		Rev X00
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SSID = VIDEO

HDMI Level Shifter & CONNECTOR



SSID = User.Interface



SSID = Thermal

Fan Connector

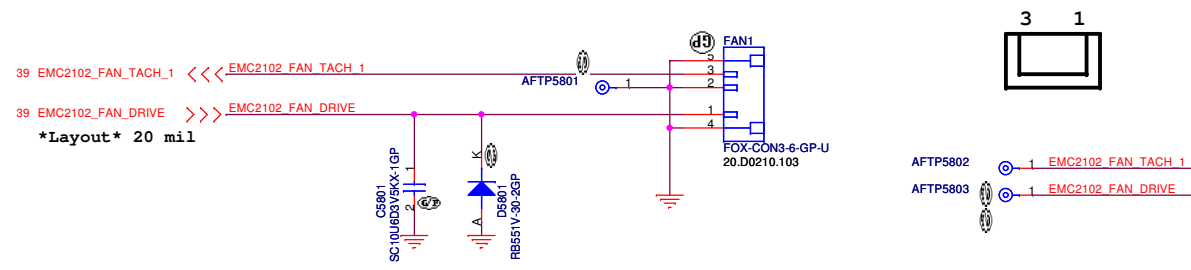


Diagram illustrating the SATA RX+ and TX+ traces for the ST210300-01 component.

The diagram shows the connection between the SATA RX+ and TX+ pins and the SATA RXN1 and TXN1 pins. The traces are labeled SCDIU0V2KX-3GP and SCDIU0V2KX-5GP.

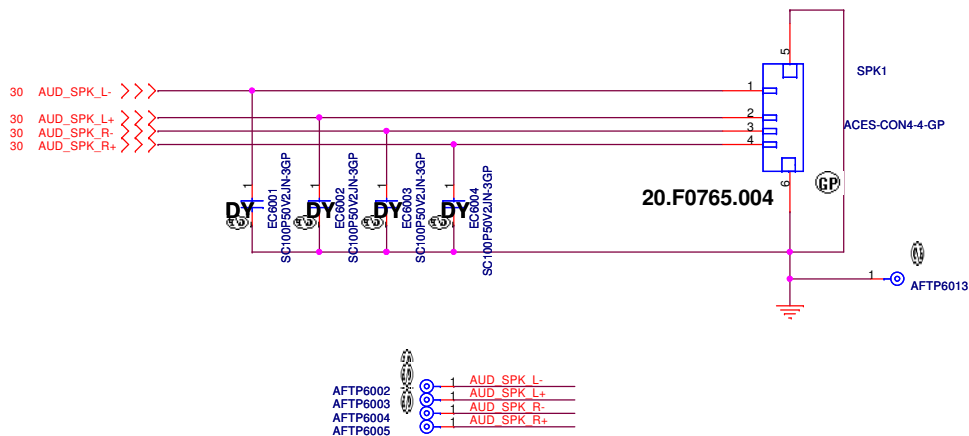
Key components and connections include:

- Power Supply:** +5V_RUN
- Ground:** GND
- Capacitors:** C5919, C5920, C5921, C5922
- Resistors:** R5902, R5901
- Traces:** SCDIU0V2KX-3GP, SCDIU0V2KX-5GP
- Pin Connections:**
 - SATA RXP1_C, SATA RXN1_C
 - SATA TXN1, SATA TXP1
 - SATA RXN1, SATA TXN1
 - SATA TXN1_DJ2, SATA TXP1_DJ2
- Component Markings:** -1_0513 DJ1
- Part Number:** SKT-SATA7P-6P-3-GP-U
- Quantity:** 22.10300-01

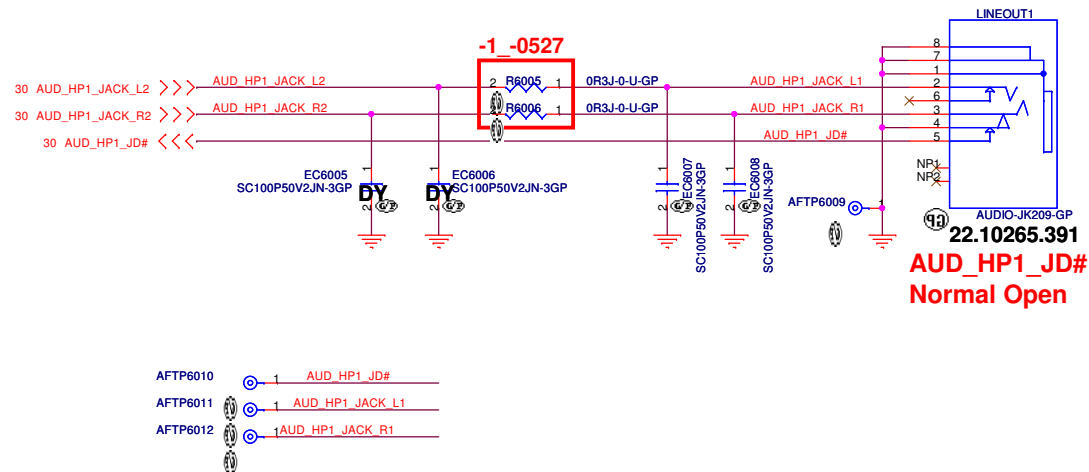
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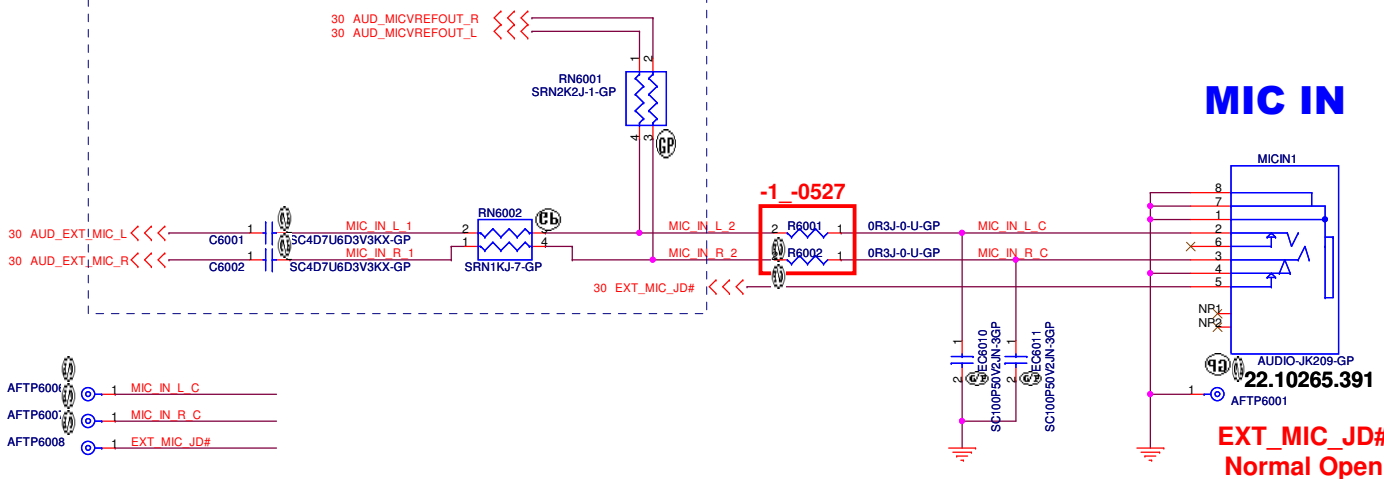
Speaker Connector



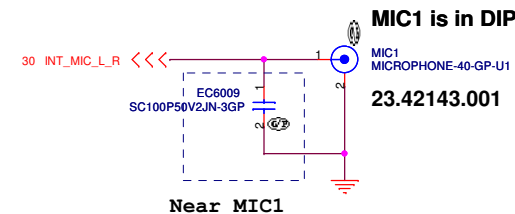
LINE1 OUT



Plase thise parts near codec



Internal Microphone



<Core Design>



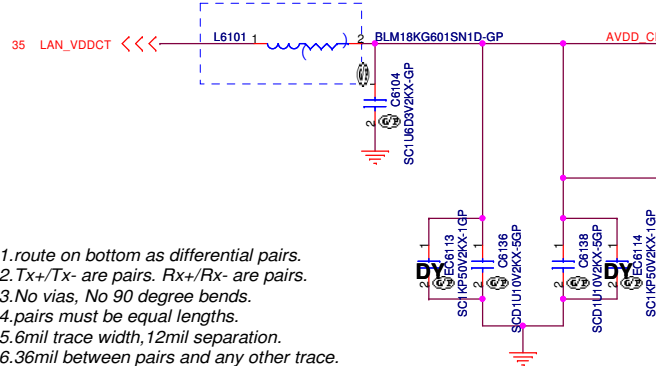
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Size	Document Number	Rev		
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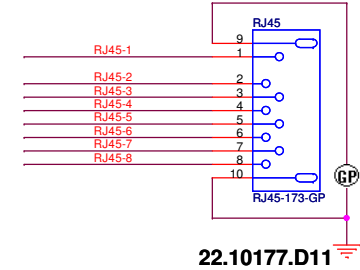
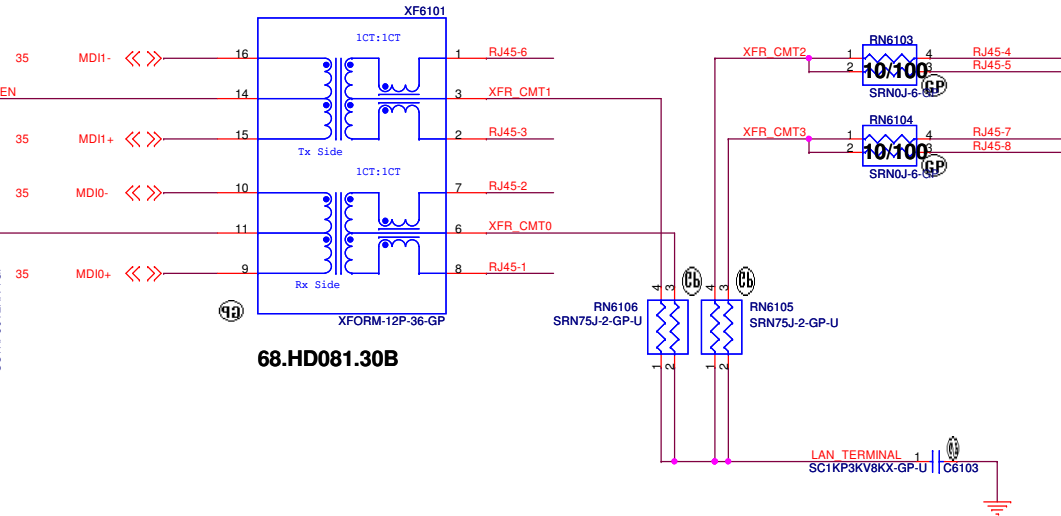
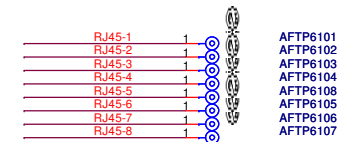
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RJ45 Connector

0603 size

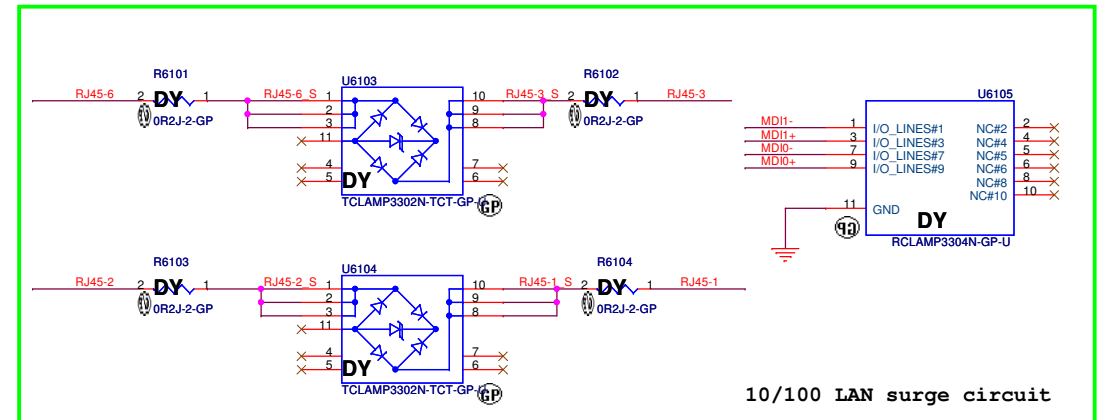


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

22.10177.D11 

The schematic diagram illustrates the internal structure of the 68.HD081.30B module. It features a central transformer with two primary windings (Tx Side and Rx Side) and two secondary windings (1CT:1CT and 1CT:1CT). The transformer is labeled 'GIGA' and 'XF6102'. The primary windings are connected to MDI2+ and MDI2- (pins 16 and 14) and MDI3+ and MDI3- (pins 15 and 10). The secondary windings are connected to RJ45-4 (pin 1), XFR_CMT2 (pin 3), RJ45-5 (pin 2), RJ45-7 (pin 7), XFR_CMT3 (pin 6), and RJ45-8 (pin 8). The transformer is also connected to AVDD_CEN (pin 11) and MDI3- (pin 9). The transformer is labeled 'XFORM-12P-36-GP'.

External components include two SC11K02KX-1GP capacitors (pins 1, 2, 3, 4) and two SC11K02KX-5GP capacitors (pins 1, 2, 3, 4). The module is labeled '68.HD081.30B'.



10/100 LAN surge circuit



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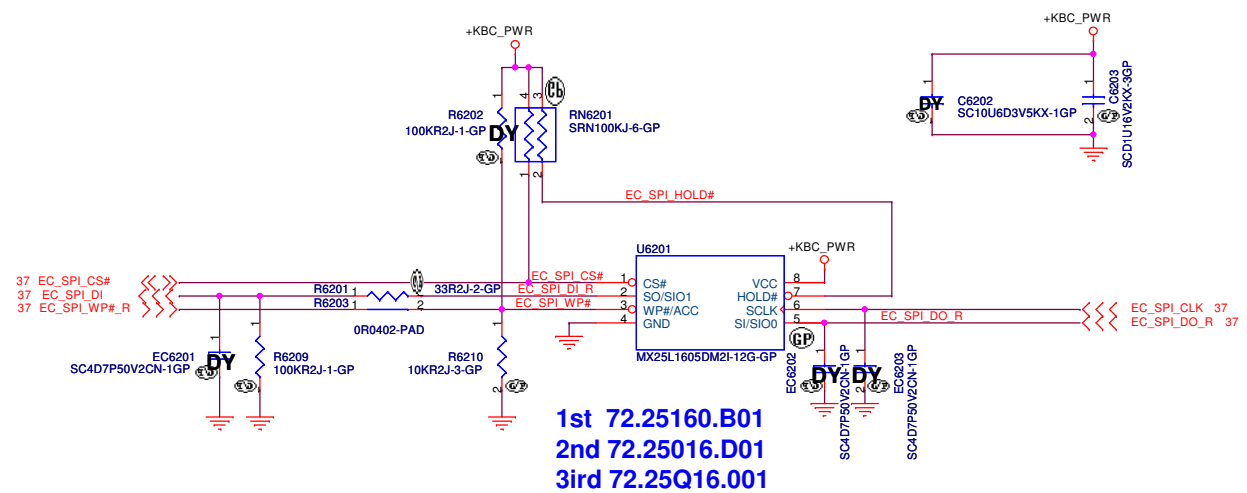
XFORM/RJ45

DJ2 Montevina UMA

Rev	X00
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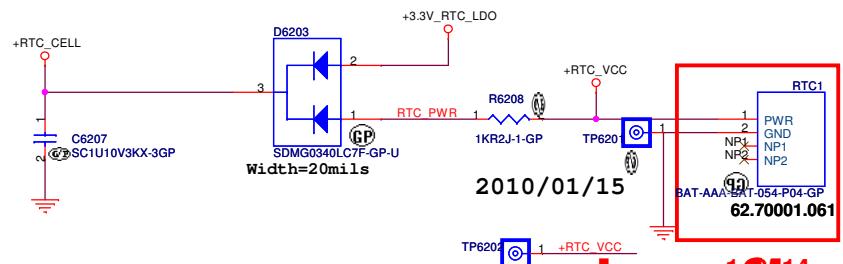
SPI FLASH ROM (16M bits) for KBC



1st 72.25160.B01
2nd 72.25016.D01
3ird 72.25Q16.001

SSID = RBATT

RTC Connector



2010/01/15

-10514

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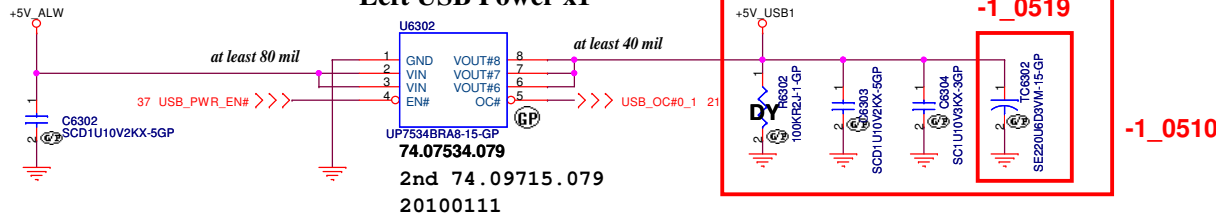
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Size: A3	Document Number: DJ2 Montevina UMA	Rev: X00
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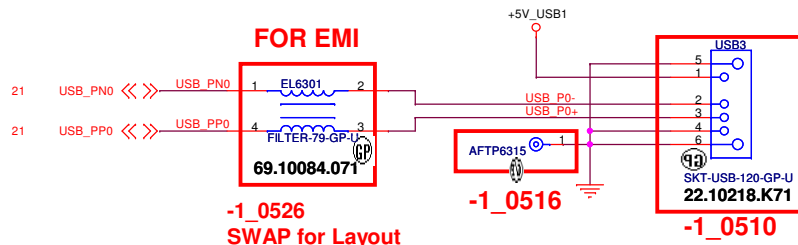
SSID = USB

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Left USB Power x1

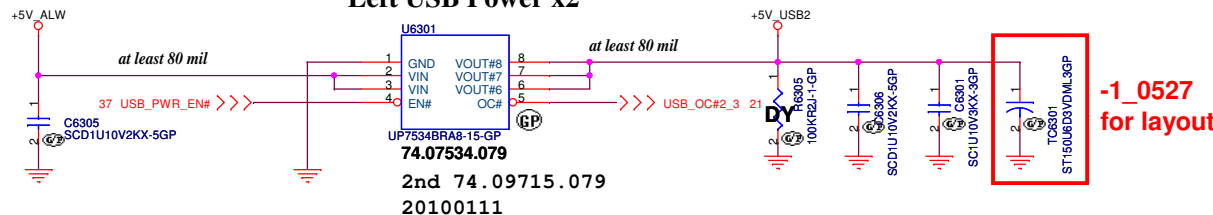


FOR EMI

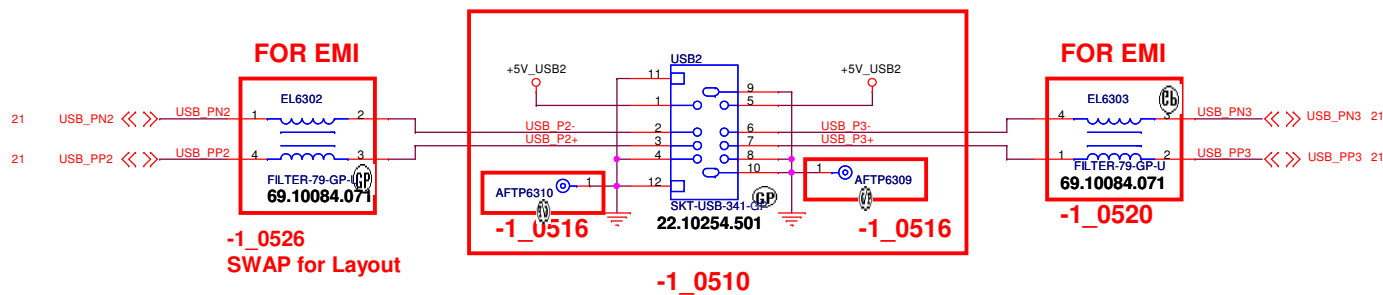


-1_0526
SWAP for Layout

Left USB Power x2



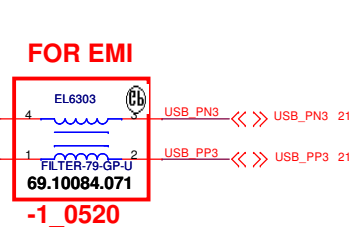
FOR EMI



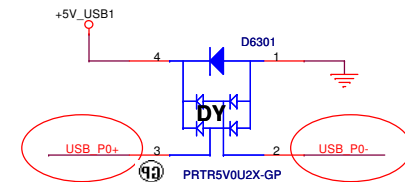
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-1_0510

FOR EMI

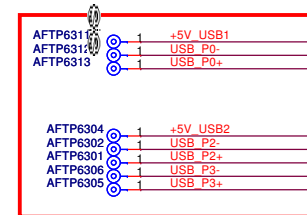


-1_0520



-1_0526
SWAP for Layout

-1_0526
remove D6302 6303 for EMI



-1_0516

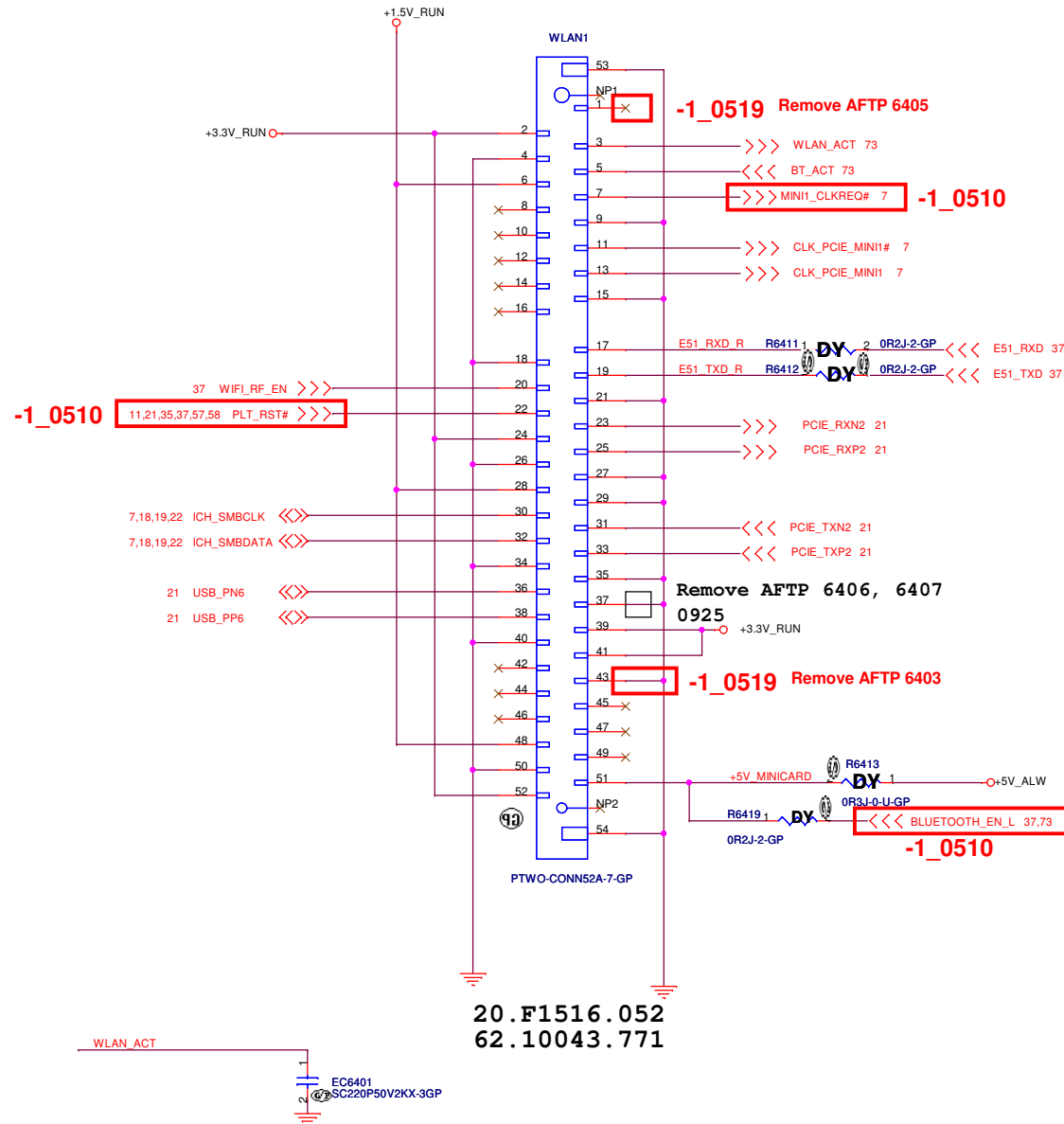
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SSID = Wireless



20.F1516.052
62.10043.771


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-1_0525



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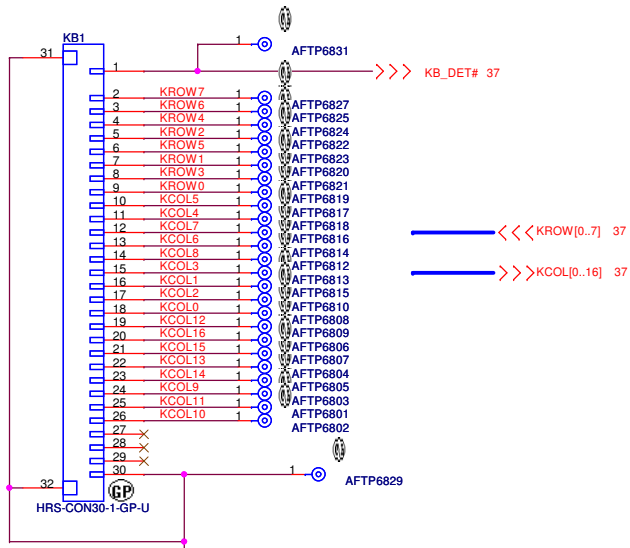
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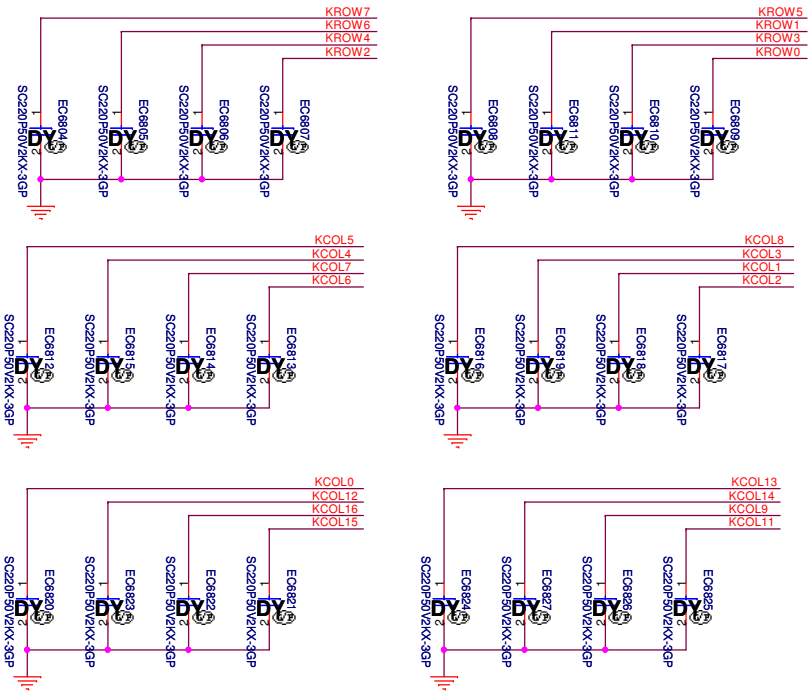
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SSID = KBC

Internal Keyboard Connector

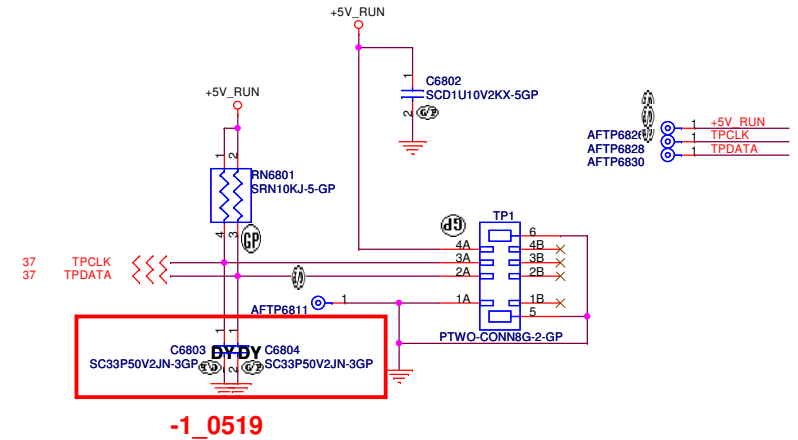


Main 20.K0421.030
20.K0259.030

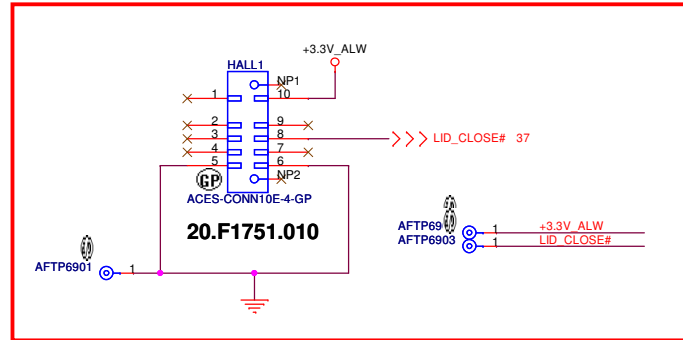


SSID = Touch.Pad

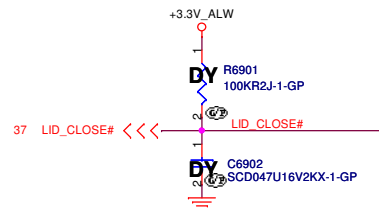
TouchPad Connector



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-1_0516

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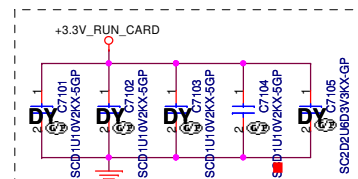
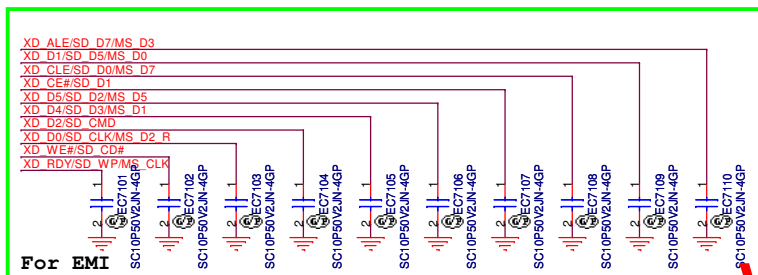
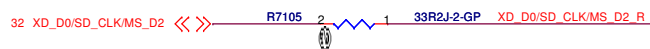
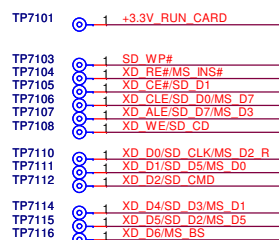
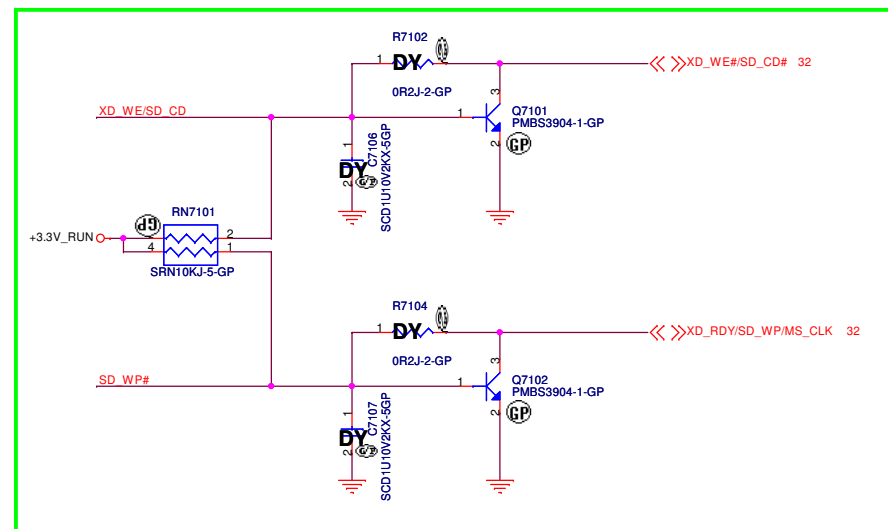
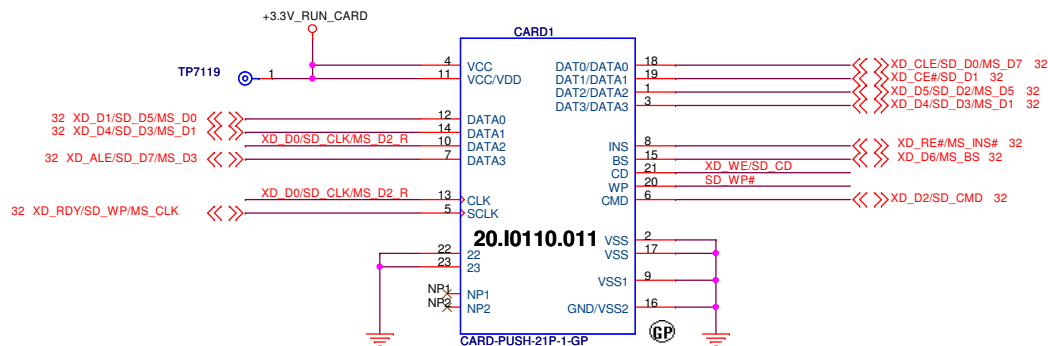
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SSID = SDIO

SD/MMC/MS Card Reader


XD_WE/SD_CD
No Card : LO
Inser Card : HI

SD_WP#
No Card : LO
Inser Card : HI



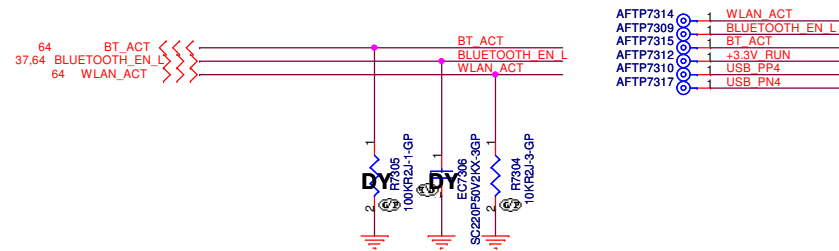
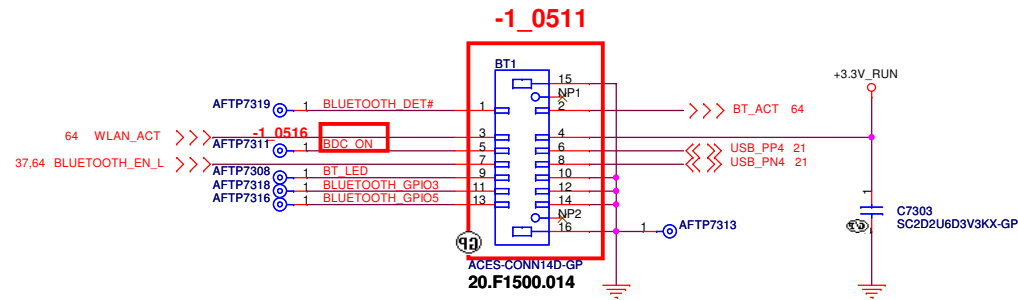
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SSID = User Interface

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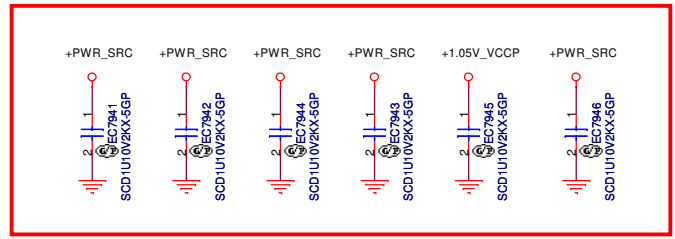
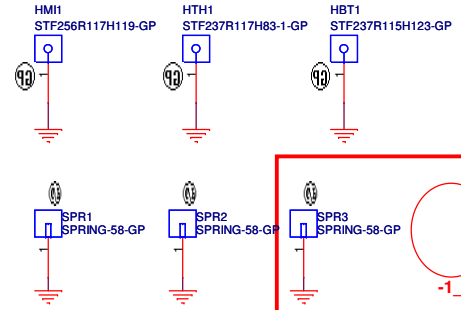
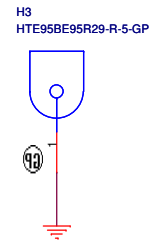
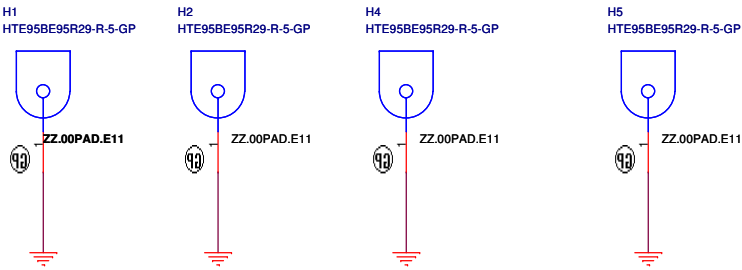
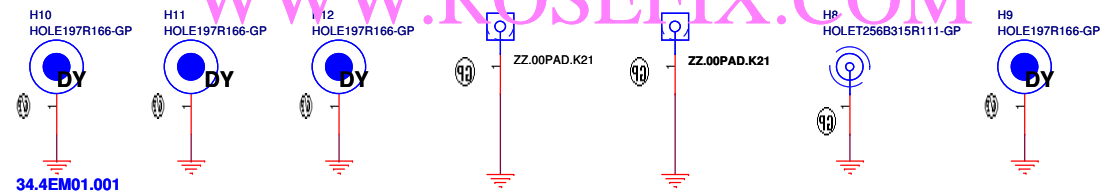
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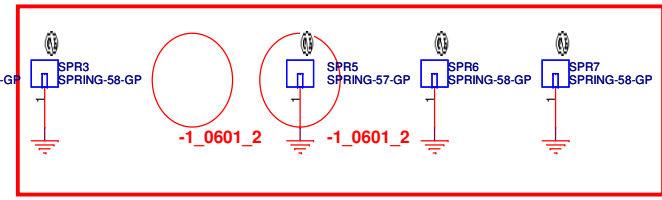
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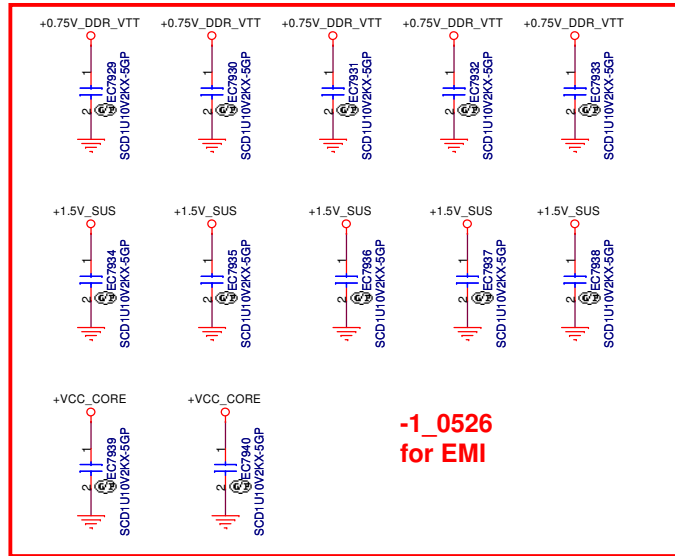
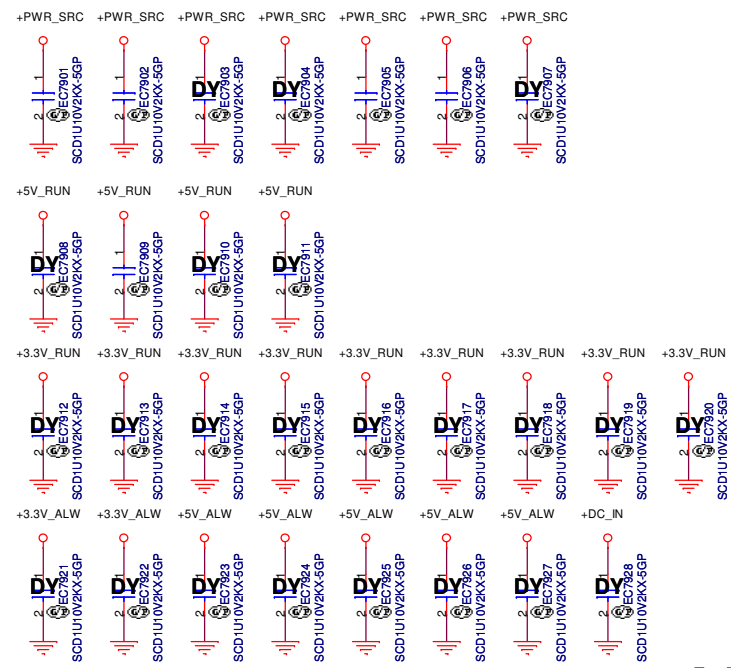
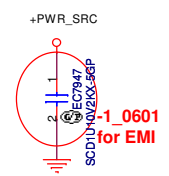
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for EMI



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